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High Speed VLSI Architecture for Parallel Counters

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***Abstract*— The aim of this paper is to design a parallel counter architecture with high operating frequency and wide range. That is achieved by partitioning the entire structure into two main parts Counting Portion(CP) and State Look-ahead Portion(SLP).The CP is partitioned to smaller bit counting sections separated by D-FF .The SLP is partitioned same way as CP. The Verilog Hardware Description Language is used for modeling the architecture. The results obtained by the synthesize tool Xilinx ISE 12.4i on a SPARTAN 3E chip demonstrate that Parallel Counter Architecture have improved operating frequency as compared to conventional synchronous counter. Coding for Parallel Counter Architecture done in Verilog HDL and simulated using ModelSim.The operating frequency is compared with conventional synchronous counters.**

***Index Terms*—Architecture Design; high-speed counter,early over flow states,FPGA**

I. INTRODUCTION

Counters are widely used for digital circuits such as frequency divider, code generator and different arithmetic operations[1].Speed enhanced counters have applications like triggering nuclear instruments and for neural networks[2]. If we require a counter with long counting width and high counting rate ,then it is desirable to design a counter that's counting rate must be independent of its width.

In early design the operating frequency of the counter is improved by partitioning the large width counter into several smaller counting sections. In which higher order sections are enabled when all bits in lower order sections are saturated[3].The drawback of this method is that initialization delay, propagation delay and decoding of AND logic will limits the operating frequency.

The speed of the counter improved by another method in which half adders are used [4]and that are enabled by carry signal from lower significance. In which the carry chain delay will limits the maximum operating frequency. Further enhancement in operating frequency achieved by reducing carry chain delay. For which a backward carry propagation technique is used[5].Another enhanced counter [6] with an aim of designing a counter with delay independent of counter width. Pre-scaling techniques are used to reduce the clock frequency .The counter is segmented in modules and high order module is clocked by low frequency signal derived by lower order modules. But extra circuit is required to detect signal in lower order bits.

II. PARALLEL COUNTER ARCITECTURE

Parallel counter structure shown in Fig.1 consists of the state look ahead portion and counting portion. The counting portion is partitioned to synchronous up counting sections and each section perform counting operations. State look ahead portion detects overflow state in each counting section and enable the higher order up counting section appropriately. This paper present 34-bit Parallel Counter Architecture [1] can configure it as 8-bit,16-bit and 32-bit according to the application.

A. Counting Portion

Counting portion of 34-bit Parallel Counter Architecture consists of three different sections. They are Section-1,Section-2,Section-3S,where S=1,2,3 etc. increasing from left to right .The bit width of section-1 depends on the bit width of the counter. Section-2 is a edge triggered DFF which is used as pipeline latches and section-3S is 2-bit synchronous up counter.Fig.2 shows the 34-bit architecture of enhanced counter.

1) Section-1 of 34-bit Parallel Counter

Section -1 of 34-bit parallel counter is a 4-bit synchronous up counter which is used for generating lower order bits of counter such as $Q_3Q_2Q_1Q_0$. This is explained in (1) which shows that the counter bit width depends on the bit width of section-1.The maximum allowable counter size (CS) is

$$CS = m + (2 * (2^m-1)) \quad (1)$$

Where m denotes the bit width of section-1.

Here m=4,then by using (1) CS become 34.Fig.3 shows hardware schematic of section-1.Which is responsible for generating early overflow states for all Section-3S in the counting portion. All the output of section-1 are used for identifying overflow.

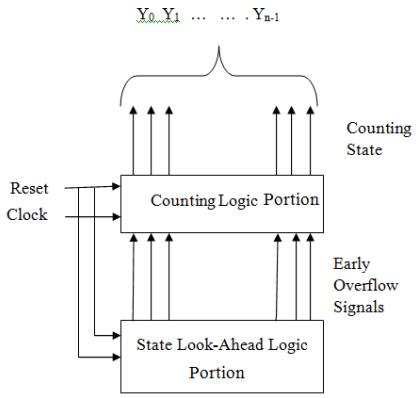


Fig. 1. Block Diagram of Parallel counter Architecture

. So that the total number of early overflow states (EO) generated by section-1 is

$$EO = 2^m - 1 \quad (2)$$

In this case EO is 15 and the overflow components (EO_Comp) required to propagate early overflow state is

$$EO\_Comp = EO - 1 \quad (3)$$

So that the architecture requires 14 states i.e upto state-14 for identifying early overflow in Enhanced counter. The output of section-1 are $Q_3Q_2Q_1Q_0$ and QEN_1,which is connected to D_{IN} of next immediate section-2.

$$QEN_1 = Q_3 \text{ AND } Q_2 \text{ AND } Q_1 \text{ AND } (\sim Q_0) \quad (4)$$

2) Section-2 of 34-bit Parallel Counter

It is a simple D-Flip Flop and it act as a delay element in the circuit. Which is present in both counting portion and state look ahead portion. In the case of counting portion the output of section-2 is used as enabling signal for next immediate section-3 but in the case of state look ahead portion which is used as early overflow state. The placement of this section in the architecture will eliminate the lengthy AND gate rippling and also the AND gate fan- in and fan-out problem present in large width counters. The number of section-2 present in the counting portion(S2_CP) of the architecture is given by (5)

$$S2\_CP = (CS - m)/2 \quad (5)$$

In this design CS = 34 and m = 4 so S2_CP become 15.That means counting portion of the architecture consists of fifteen number of section-2's.

3) Section-3S of 34-bit Parallel Counter

It is a parallel synchronous binary 2-bit counter whose count is enabled by INS signal which is coming from the output of preceding section-2.

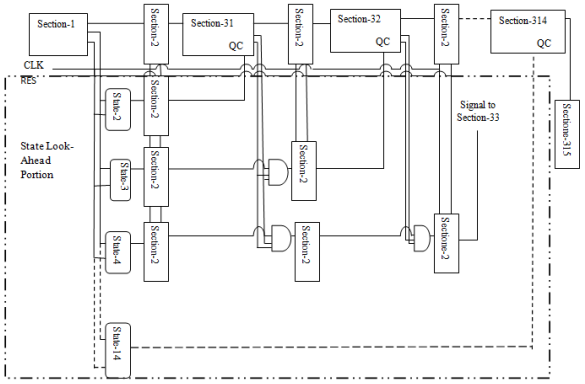


Fig. 2. Functional Diagram of Parallel counter Architecture

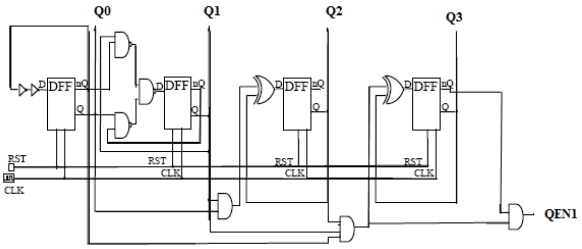


Fig. 3. Schematic of Section-1

The schematic diagram of section-3 is shown in fig.4.The output of section-3 are Q_1 Q_0 and QEN3,which is connected to next immediate section-2 as its input.

$$QEN_3 = QC \text{ AND } Q_1 \text{ AND } Q_0 \quad (6)$$

Where QC is the signal coming from state look ahead portion.

The number of section-3S in CP(S3_CP) is equal to that of section-2 in CP. So here S3_CP=15.Total number of components for the design is specified in the table 1.

B. State Look -Ahead Portion

The SLP trigger the higher order states by decoding the lower order count states and which is carrying over several clock cycles. That is equivalent to one cycle look-ahead mechanism. The use of SLP in design will avoid the overhead delay detector circuits in large width counter. The SLP select different states of section-1 and then introduce suitable delay or pipeline latches depending upon the order of section-3S. Total number of section-2 in SLP(S2_SLP) is

$$S2\_SLP = ((CS - m)/2 - 1)\,((CS - m)/2 - 1) + 1)/2 \quad (7)$$

Where CS is Counter Size & m is bit width of Section-1

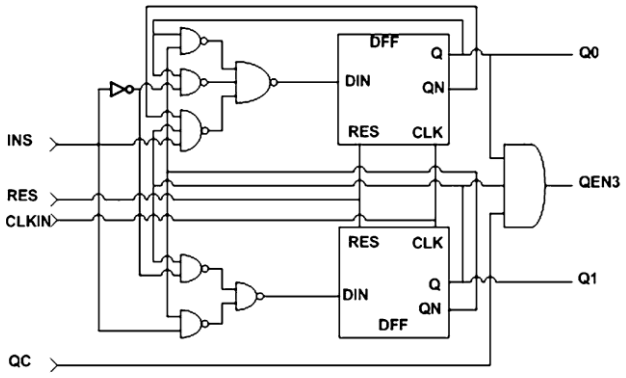


Fig. 4. Schematic of Section-3

TABLE I. NUMBER OF COMPONENTS

Component	Section-1 Size		
	m=2-bit	*m=3-bit*	*m=4-bit*
CS	8	17	34
M3_CP	3	7	15
M2	6	28	120
EO_ Comp	2	6	14

So the total number of section-2 in the overall design(S2) is

$$S2=S2\_CP+S2\_SLP \quad (8)$$

For example ,in a 34-bit parallel counter the width of section-1 is 4bit.So it have 16 count state in which the enhanced counter can identifies the overflow in fifteen ways.In which when section-1 output reaches $Q_3Q_2Q_1Q_0$ = 1110 section-2 decode this state and carries this across one clock cycle and enable Q_5Q_4 = 01 at section - 31 on the next rising clock edge.

This process is repeated upto the saturation of section-31.For enabling next section-3 i.e section-32 the design identifies overflow before two clock at $Q_3Q_2Q_1Q_0$ = 1101 and is pipelined across two clock cycles.When Q_5Q_4 = 11 and the signal QC of section-31 is active then it will enable the section-32 on next rising clock edge.Thus the early overflow pipelining through SLP is used for enabling higher order bits.This organization enables all the sections in the design cuncurrently on the clock edge and avoid the long frequency delay.

III. RESULTS

In this section we present simulation and synthesis result for the 34-bit enhanced counter. Functional verification is done by using HDL representation and is simulated using the tool ModelSim. The design synthesized using Xilinx ISE.

A. Simulation Results

Parallel Counter Architecture have the advantage of improved operating frequency. In this project operating frequency of this design is compared with that of conventional counter. This 34-bit parallel counter have three different sections (Section-1,section-2,section-3S).Simulation of each section done independently.

1) Section-1

In the case of 34-bit parallel counter the section-1 have a size of 4-bit.When the reset input become LOW then the 4 bit counter starts count from 0 to 15 . The simulation wave form shown in fig.5.When it reaches terminal count 15 then it again starts from 0 and repeat the counting. When the counter reaches the count 1110 then the '**qen1**' output of Module-1 become HIGH .Which is the count enable input for the next Module. When the qen1 become HIGH ,then the next Module immediate to Module-1 will starts counting at next clock pulse.

2) Section-2

Section-2 is a DFF and is only act as a delay element in the design. Output of this section is used as enable signal for section-3S.Simulation waveform shown in fig.6.

3) Section-3

The functioning of Section-3 is in response to the status of INS and QC input. Even though the reset become active, if the INS is low then the circuit will not starts working. So whenever the INS become active the Section-3 starts its working as a 2-bit up counter. The INS input is the output of previous Section in Counting Portion which is activated at correct time to enable next section. The QC input is the stimulus from State Look Ahead Portion,QEN3 the output of Section-3 to enable next section become active when the count reaches'11' and the QC become HIGH.Simulation waveform shown in fig.7.

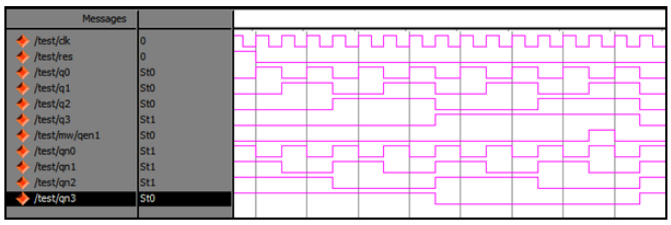


Fig.5. Output waveform of section-1

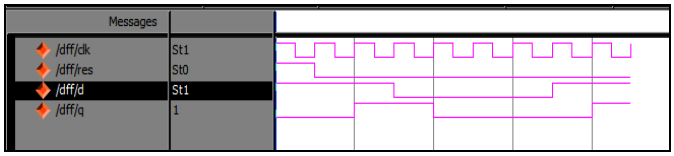


Fig. 6. Output Waveform of Section-2

Fig. 7. Output waveform of Section-3

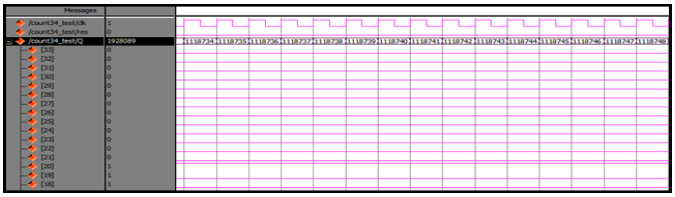
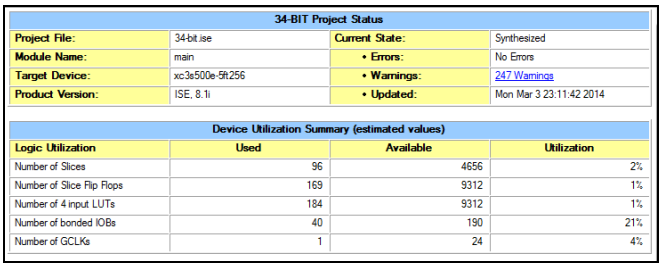


Fig. 8. Output waveform of 34-bit parallel counter (bit 18-bit 33)

B. Synthesis Result

Parallel Counter architecture is synthesized on Spartan 3E XC 3S 500E-ft 256 using the tool Xilinx ISE 8.1i . Synthesize result is shown in fig.9.



34-BIT Project Status

Project File:	34-bit ise	Current State:	Synthesized
Module Name:	main	• Errors:	No Errors
Target Device:	xc3s500e-5ft256	• Warnings:	247 Warnings
Product Version:	ISE, 8.1i	• Updated:	Mon Mar 3 23:11:42 2014

Device Utilization Summary (estimated values)

Logic Utilization	Used	Available	Utilization
Number of Slices	96	4656	2%
Number of Slice Flip Flops	169	9312	1%
Number of 4 input LUTs	184	9312	1%
Number of bonded IOBs	40	190	21%
Number of GCLKs	1	24	4%

Fig. 9. Synthesis Report of 34-bit Parallel Counter

TABLE II. COMPARISON RESULT

Parameter	**34-bitParallel Counter**	**34-bit Conventional Synchronous Counter**
Minimum Clock Period(ns)	8.6	9.8
Maximum Operating Frequency(MHz)	115	101

By examining the minimum clock period for the Parallel counter we can realize that the value is less than that of conventional synchronous counter. Comparison of operating frequency is shown in table II. We can say that operating frequency of this Parallel Counter is high as compared to Conventional Synchronous Counter.

IV . CONCLUSION

The main feature of Parallel Counter Architecture is that it has a pipelined structure .The State Look ahead portion in the architecture helps to activate all sections concurrently with out any rippling effect. In addition this structure avoids using a long chain detector circuit typically required for large width counters. This structure uses a regular VLSI topology which is attractive for continued technology scaling due to two repeated module types.

Future work involve further enhancement of speed which is possible using various advanced design techniques for each Sections. Also research is going on for further refining of results and improvement of design for more complex circuits and systems. The maximum clock speed is a design parameter of primary importance if it is used for timing application such as generation of timi9ng pulse for optical instrumentation.

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