A Multilevel Converter with a Floating Bridge for Open-End Winding Motor Drive

B.Reshma [1], B.Sathyavani[2]
M.Tech student P.E, EEE, SR Engineering College, Warangal, Telangana, India
Assistant professor, EEE, SR Engineering College, Warangal, Telangana, India

Abstract- **In this paper, a circuit topology is analyzed, which is used as a three-level open-end winding IM drive. This topology uses dual inverters with only one dc voltage source at the primary side of the converter. The second bridge converter is connected to a floating capacitor bank. The aim of this topology is to eliminate the requirement for a bulky isolation transformer while achieving multilevel output voltage waveforms. The voltage across the floating capacitor bank is controlled using the redundant switching vectors along with a modified space vector modulation (SVM) scheme, which avoids unwanted voltage levels.**

Index Terms- **Field-oriented control (FOC), floating bridge, open-end winding induction machine, space vector.**

I. INTRODUCTION

In the past few years multilevel converters are identified as a preferred topology for high energy uses as a result of benefits like high amounts of modularity, accessibility, general efficiency, and high production waveform quality. This is attained at the cost of increased numbers of pieces and control complexity [1] [3]. In electrical traction drives multilevel inverters have been effectively applied in order to develop system reliability and minimize failures on motor windings as a consequence of the lower typical mode voltages that they create [four], [5]. Precisely the same benefits could be achieved when used to Hybrid Electric Vehicles. Along with this functionality, if the dc side is actually attached to a pair of batteries or perhaps some other power storage products the multilevel converter can be used to keep the charge sense of balance of the big energy storage system [6, [7]. Multilevel converters are also applied for power quality improvement as well as Facts exactly where, especially in aerospace programs, the diminished filtering requirement required for multilevel converter represents an edge in phrases of total converter excess weight and cost [8]. Also we have observed in this years, multilevel converters are actually likely to end up used increasingly in electric power grids to be able to attain a greater flexibility and reliability &amp allow sensible energy management in the presence of various sources of energy and utilities hooked up to the grid. A good example is actually the replacement of distribution amount substation transformers with higher energy multilevel back-to-back converters.

However, the balancing of the DC-Link voltages represents an issue for the DCM strategy as such a technique is able to passively balance the DC Link voltages only when balanced dc currents are demanded. Moreover, in the DCM technique, the devices voltage drops and on-state resistances are not considered. In order to overcome these issues, an active DC-Link voltage balancing algorithm has been designed for DCM which accounts for the device voltage drops and on-state resistances, improving the output voltage waveform quality and maintaining good performances even when unbalanced dc currents are demanded. In the concept of DC-Link voltage balancing algorithm is introduced as well as the device voltage drop and on-state resistance compensation. The main target of the proposed modulation strategy is, in contrast with DCM, to minimize the DC-Link voltage unbalance among the different converter cells in order to maintain the converter modularity and produce high quality waveforms, even if a low switching frequency is considered.

In this paper, a circuit topology is analyzed, which is used as a three-level open-end winding IM drive. This topology uses dual inverters with only one dc voltage source at the primary side of the converter. The second bridge converter is connected to a floating capacitor bank. The aim of this topology is to eliminate the requirement for a bulky isolation transformer while achieving multilevel output voltage waveforms. The voltage across the floating capacitor bank is controlled using the redundant switching vectors along with a modified space vector modulation (SVM) scheme, which avoids unwanted voltage levels in the phase voltage waveforms during the dead-time intervals, thus improving the overall waveform quality.

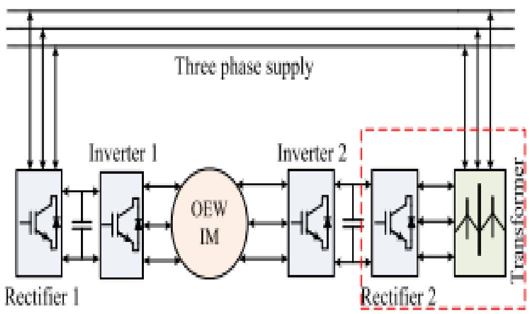

Fig. 1 *Conventional open-end winding IM drive topology*

II. PROPOSED CONTROL STRATEGY

The floating bridge capacitor dual-inverter based topology has been analyzed for different applications. The topology can be used to supply reactive power to a machine and to compensate for any supply voltage droop, but the possibility of multilevel output voltage waveforms was not considered. A control scheme to charge the floating capacitor bridge along with multilevel output voltage waveforms has been presented. In this method, the main converter works in a six-step mode and the floating converter is called conditioning inverter as it is improving the waveform quality.

The work described in this paper is to control the voltage across the floating inverter bridge capacitor using the redundant switching states, therefore removing the need for any isolation transformer and allowing the converter to achieve multilevel output voltage waveforms. Fig. 2 shows a block diagram of the dual inverter with a floating bridge and associated capacitor.

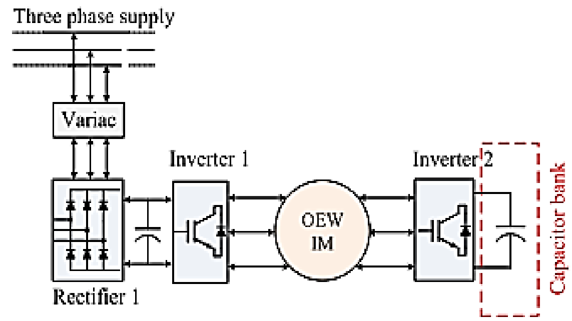

Fig.2 *Block diagram of the proposed floating bridge topology.*

The use of a dc-link voltage ratio of 2:1 allows the dual-bridge inverter to produce up to a three levels in the output voltage waveform. The power stage of the proposed topology is shown in Fig. 3.

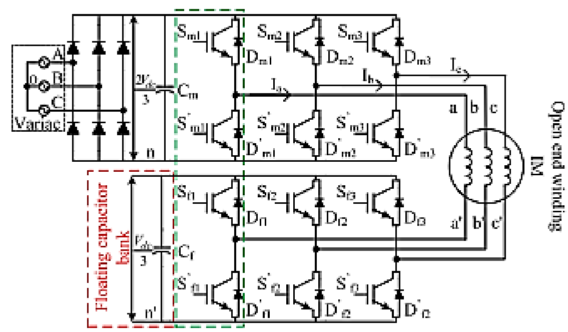

Fig.3 *Power stage of the floating bridge topology (the floating capacitor is charged to half of the main dc-link voltage)*

In order to show how the floating capacitor can be charged and discharged, the possible switching states are analyzed. The space vector diagram for the topology is shown in Fig. 4, which is derived by assuming that both converters are supplied from isolated dc sources with a voltage ratio of 2:1. As in Fig.4, the red numbered switching combinations discharge the floating capacitor, while the green numbered switching combinations charge the floating capacitor. The blue numbered switching combinations hold the last state of capacitor and are, therefore, neutral in terms of the state of charge of the floating capacitor. As an example state shown in Fig. 5 gives the switching sequences for both converter's top switches, 7(1 1 1) represents the top three switches for main inverter and 4 (0 1 1) represents the switching states for top three switches of the floating converter.

It can be seen from Fig. 5 that combinations (11) and (16) will direct the current through the positive to negative terminal of the floating capacitor and thus will act to charge the capacitor. Combinations (14), (15), and (74) will result in a current in the other direction and will, therefore, act to discharge the capacitor. Combinations ending with 7 (1 1 1) or 8 (0 0 0) are zero states and will, therefore, have no impact of floating capacitor's voltage.

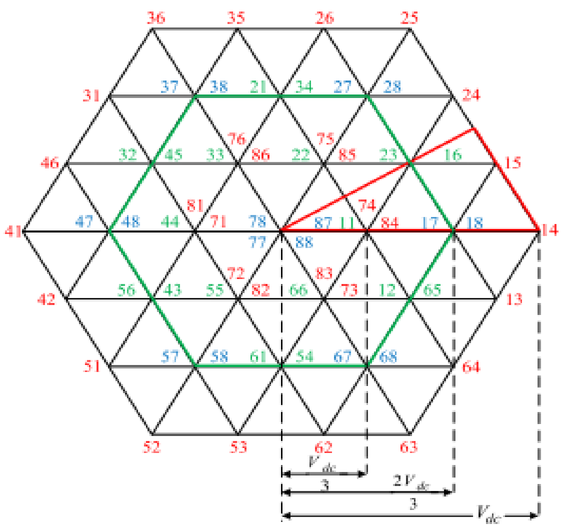

Fig. 4 *Space vector of dual two-level inverter (source ratio 2:1)*

It is evident from Fig. 4 that if the reference voltage is in outer hexagon, then there are only two switching combinations in each sector to charge the floating capacitor. During inductive load operation, capacitor discharge rate will be slower and will cause overcharging if the reference voltage lies in outer hexagon. Also, due to lack of charging states, the floating capacitor will discharge if the machine is drawing active power. To avoid these two phenomena, a restriction has to be imposed on modulation index. As a result, the maximum useable number of voltage levels across the load will be reduced to nine (13 for isolated sources) along with a slightly lower than ideal dc bus voltage utilization. Therefore, the floating capacitor can charge to half of the main dc-link capacitor voltage only if the modulation index (m) is limited as shown in the following:

m = 0.66…………………………… (1)

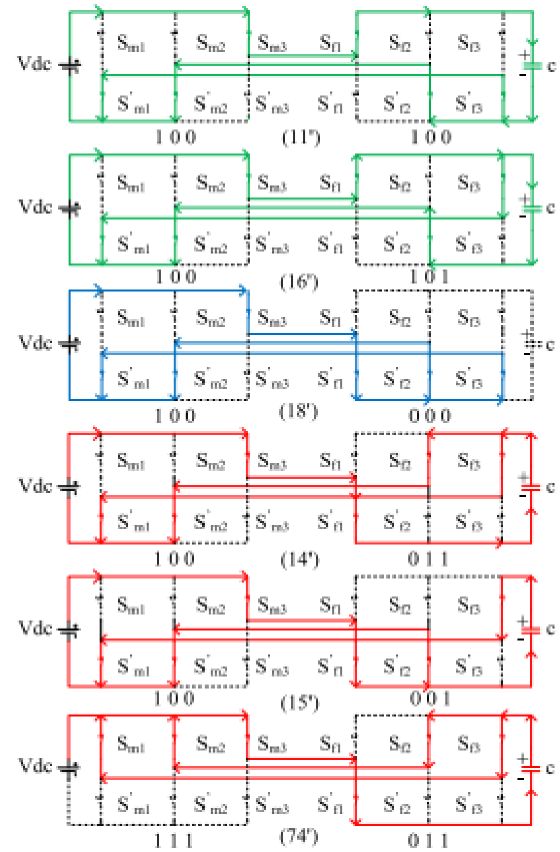

Fig. 5 *Current flow for different switching state*

This is 33% reduction of dc bus utilization in contrast with a dual inverter supplied by two isolated sources.

A. *Modulation Strategy*

A decoupled space vector modulation strategy has been used for this dual-inverter floating bridge topology. Switching combinations are selected in such a way that the average generated voltage for each of the converters is 180° phase shifted from the other [see Fig. 6(a)]. These voltages will then add up at load terminal to match overall voltage reference [see Fig. 6(b)]. Identification of the subsectors, dwell time calculation, and the switching sequence design can be found. To achieve better results, the output switching sequences are modified. The modification of the pulses is necessary to minimize the unwanted voltage **Modulation Strategy:** A decoupled space vector modulation strategy has been used for this dual-inverter floating bridge topology. Switching combinations are selected in such a way that the average generated voltage for each of the converters is 180° phase shifted from the other [see Fig. 6(a)]. These voltages will then add up at load terminal to match overall voltage reference [see Fig. 6(b)]. Identification of the subsectors, dwell time calculation, and the switching sequence design can be found. To achieve better results, the output switching sequences are modified. The modification of the pulses is necessary to minimize the unwanted voltage

A generalized solution is shown in Fig. 7 for positive load current. It can be seen from Fig.7 that the pulses are delayed depending on the switching states transitions. Due to the modified switching sequences, the current direction does not change during the dead-time. The state of the floating capacitor will depend on the current just before the occurrence of dead-time interval. As an example, if the capacitor was charging, then it will keep charging when the converter is in dead-time period. The value of dead-time is too small for any overcharge or discharge to change the capacitor voltage drastically.

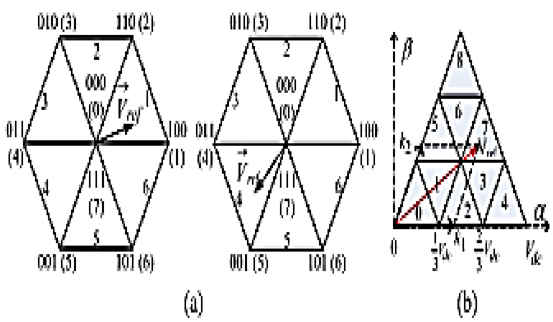

Fig.6 *(a) Space vector diagram of individual converter (not in scale). (b) Space vector diagram of the dual-inverter system with source ratio*

B. Advantages

1) This topology is to eliminate the requirement for a bulky isolation transformer whilst achieving multi-level output voltage waveforms.
2) The voltage across the floating capacitor bank is controlled using the redundant switching vectors along with a modified SVM scheme which avoids unwanted voltage levels in the phase voltage waveforms during the dead-time intervals, thus improving the overall waveform quality.

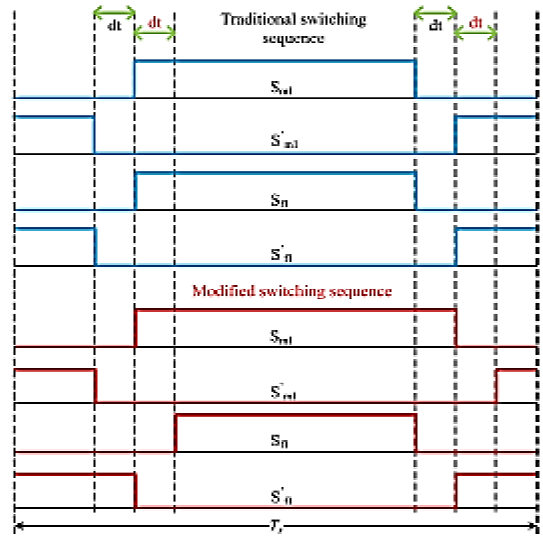

Fig. 7 *Delayed dead-time intervals in both converters when current direction is positive*

C. Applications

1) High power or low voltage, high frequency applications.
2) And also used in agriculture loads.

III. SIMULATION AND RESULTS

The proposed modulation scheme has been simulated using MATLAB and PLECS. Fig. 9 shows the charging and discharging of floating capacitor voltage. To obtain a multilevel inverter topology main bridge inverter is supplied with 260 V dc and then the floating capacitor is charged to 130V. The system is connected to an open phase R-L load.

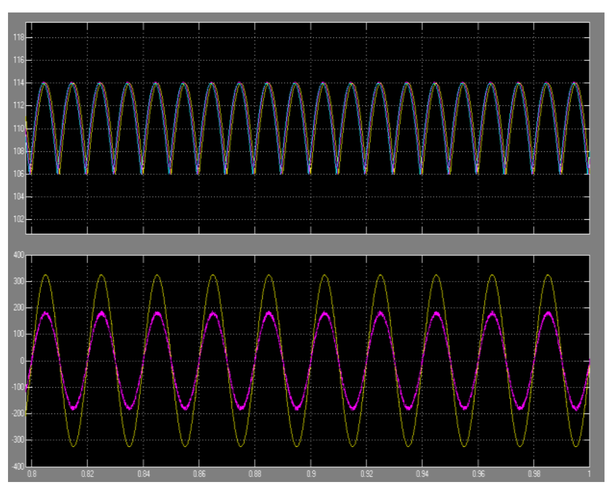

Fig. 8

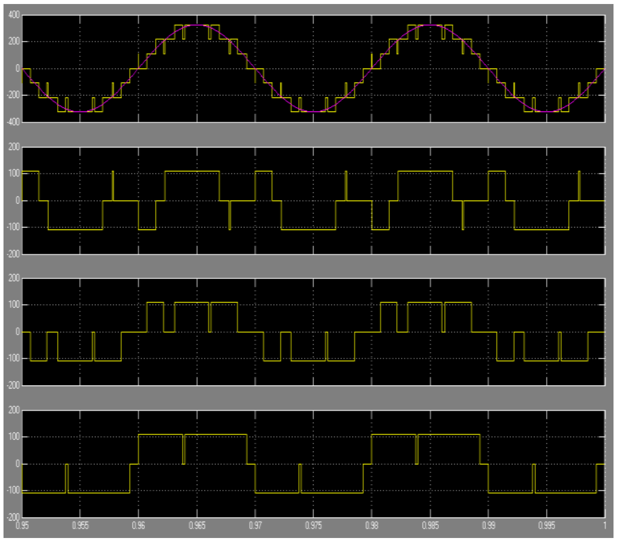

Fig. 9

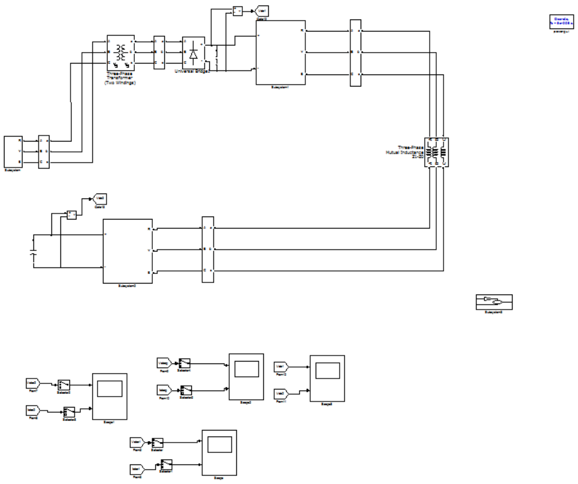

Fig. 10

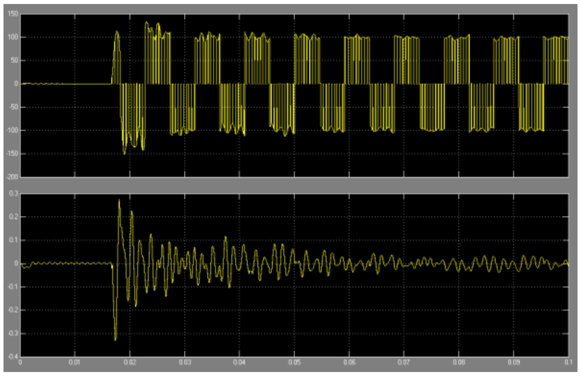

Fig. 11

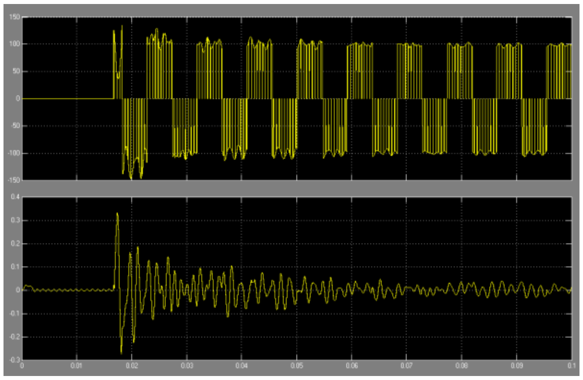

Fig. 12

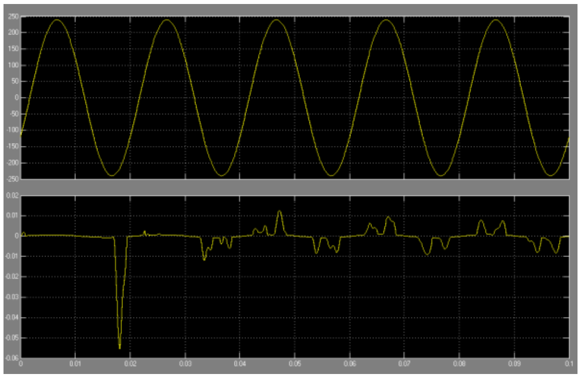

Fig. 13

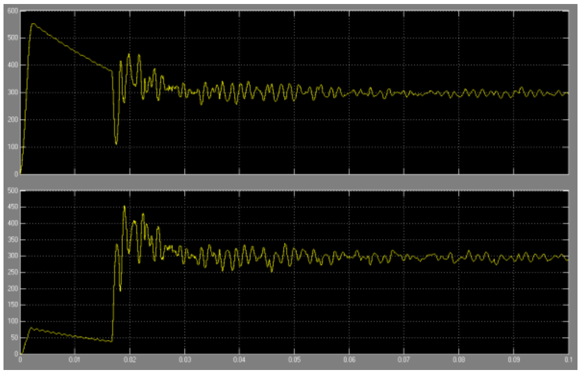

Fig. 14

The converter to achieve output waveforms Fig:10 shows the simulation block diagram. Fig: 11. Shows the second inverter and Fig:12. Shows the first inverter output waveform. Fig:14 shows input voltage waveforms of dual inverter .Fig:13 shows the combination of the input and output waveforms of dual inverter.

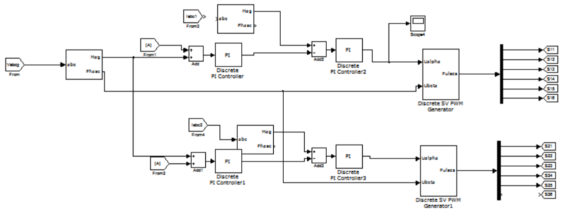

Fig. 15 *PI controller of the system*

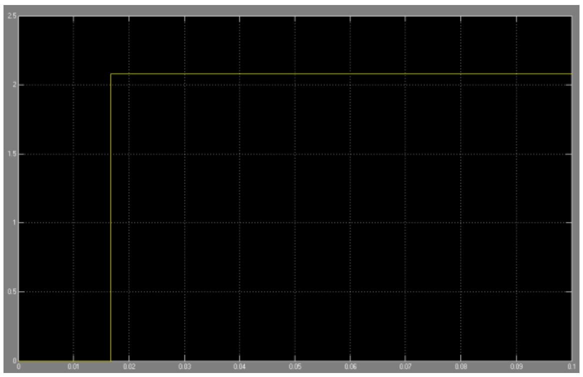

Fig. 16 *PI controller of the system*

IV. CONCLUSION

A motor drive utilizing an amenable stator winding induction machine along with a dual-bridge inverter topology having a floating capacitor bridge has been examined, as well as pragmatic results are actually demon- strated. The proposed method energizes the floating bridge capacitor to a ratio of 2:1 with appreciate to primary bridge dc-link voltage amplitude. This specific dc-link voltage ratio allows the converter to get multilevel result voltage waveform. The floating dc-link voltage is actually maintained at a continuous voltage by the ways of recharging as well as discharging the floating bridge capacitor. This's attained by choosing between the charging and discharging unwanted states of this converter.

REFERENCES

[1] P. Wheeler, L. Xu, L. Meng Yeong, L. Empringham, C. Klumpner, and J. Clare, "A review of multi-level matrix converter topologies," in Proc. 4th IET Conf. Power Electron., Mach. Drives, 2008, pp. 286–290.

[2] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[4] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[5] D. Janik, T. Kosan, P. Kamenicky, and Z. Peroutka, "Universal precharging method for dc-link and flying capacitors of four-level flying capacitor converter," in Proc. Annu. Conf. IEEE Ind. Electron. Soc., 2013, pp. 6322–6327.

[6] E. C. Dos Santos, F. Gulpinar, and E. R. C. Da Silva, "Flying capacitor four-level H-bridge converter," in Proc. Power Energy Conf. Illinois, 2014, pp. 1–6.

[7] E. Levi, "Multiphase electric machines for variable-speed applications," IEEE Trans. Ind. Electron., vol. 55, no. 5, pp. 1893–1909, May 2008.

[8] S. Kouro, J. Rodriguez, W. Bin, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," IEEE Ind. Appl. Mag., vol. 18, no. 4, pp. 26–39, Jul./Aug. 2012.

[9] F. Betin et al., "Trends in electrical machines control: Samples for classical, sensorless, and fault-tolerant techniques," IEEE Ind. Electron. Mag., vol. 8, no. 2, pp. 43–55, Jun. 2014.

[10] F. Meinguet, N. Ngac-Ky, P. Sandulescu, X. Kestelyn, and E. Semail, "Fault-tolerant operation of an open-end winding five-phase PMSM drive with inverter faults," in Proc. Annu. Conf. IEEE Ind. Electron. Soc., 2013, pp. 5191–5196.

[11] N. Ertugrul, W. Soong, G. Dostal, and D. Saxon, “Fault tolerant motor drive system with redundancy for critical applications,” in Proc. IEEE Power Electron. Spec. Conf., 2002, vol. 3, pp. 1457–1462.

[12] O. A. Taha and M. Pacas, “Hardware implementation of balance control for three-phase grid connection 5-level cascaded H-bridge converter using DSP,” in Proc. IEEE Int. Symp. Ind. Electron., 2014, pp. 1366–1371

[13] S. Jae Hyeong, C. Chang-Ho, and H. Dong-Seok, “A new simplified space-vector PWM method for three-level inverters,” IEEE Trans. Power Electron., vol. 16, no. 4, pp. 545–550, Jul. 2001.

[14] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, “Fault tolerant three-phase AC motor drive topologies: A comparison of features, cost, and limitations,” IEEE Trans. Power Electron., vol. 19, no. 4, pp. 1108–1116, Jul. 2004.

[15] N. Bodo, M. Jones, and E. Levi, “PWM techniques for an open-end winding fivephase drive with a single DC source supply,” in Proc. Annu. Conf. IEEE Ind. Electron. Soc., 2012, pp. 3641–3646.

[16] E. Levi, M. Jones, and W. Satiawan, “A multiphase dual-inverter supplied drive structure for electric and hybrid electric vehicles,” in Proc. IEEE Veh. Power Propul. Conf., 2010, pp. 1–7.

[17] K. Ramachandrasekhar, S. Mohan, and S. Srinivas, “An improved PWM for a dual two-level inverter fed open-end winding induction motor drive,” in Proc. Int. Conf. Elect. Mach., 2010, pp. 1–6.

[18] E. G. Shivakumar, K. Gopakumar, S. K. Sinha, A. Pittet, and V. T. Ranganathan, “Space vector PWM control of dual inverter fed open-end winding induction motor drive,” in Proc. IEEE Appl. Power Electron. Conf. Expo., 2001, vol. 1, pp. 399–405.

[19] V. T. Somasekhar, K. Gopakumar, A. Pittet, and V. T. Ranganathan, “A novel PWM inverter switching strategy for a dual two-level inverter fed open-end winding induction motor drive,” in Proc. IEEE Int. Conf. Power Electron. Drive Syst., 2001, vol. 1, pp. 196–202.

[20] Y. Zhao and T. A. Lipo, “Space vector PWM control of dual three-phase induction machine using vector space decomposition,” IEEE Trans. Ind. Appl., vol. 31, no. 5, pp. 1100–1109, Sep./Oct. 1995.