Design a Low Power sram Architecture Based on Finfet Technology

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***Abstract*- Basically, the average 8T-SRAM does not need any write back scheme. But it has a competitive area. The average 8T SRAM architecture consists of full swing local bit line (BL). This bit line is connected to the gate of read buffer. This read buffer is obtained by boosted word line voltage (WL). The average 8T-SRAM is based on the advanced technology that is 22-nm FinFET technology. But in this 22 nm FinFET technology we do not use the word line voltage because it degrades the stability of SRAM. If it degrades the stability then gate of read buffer cannot exerts through the supply voltages then lager delays will occur in the SRAM. To overcome this differential SRAM technology is introduced. In this SRAM proposed architecture, by using cross coupled pMOSs the full swing of local bit lines are exerted and coming to the gate of read buffer, it exerts from a full vdd. This proposed SRAM architectures stores the multiple bits. Now this multiple bits examine from the minimum operating voltage and area per bit. Basically in one block this proposed SRAM stores four bits and obtains minimum voltage of 0.42v.Compared to the average-8T SRAM based on the 22-nm FinFET technology, the proposed SRAM architecture produces time delay less than 62.6.**

I. INTRODUCTION

Generally in battery powered applications like handled smart devices and implant medical devices the low power operations are the major problems associated with system on chip (SOC). Later this low power system on chips is realized with the low power static random access memory. In this SRAM affects the total power of SOC and occupies the large portion of area of SOC. Because of this there is reduction in power and low operating voltage effects the variations in threshold voltage.

To obtain high density integration, in SRAM cell small transistors are used. Coming to the 6T SRAM, it consists of both read and writes stability in low voltage region. The main advantage of adding decoupled read port is that it eliminates the tradeoff between read stability and write stability. There are soft errors occurred in the SRAM cell, to elimatete these errors we use the bit interleaving SRAM architecture.

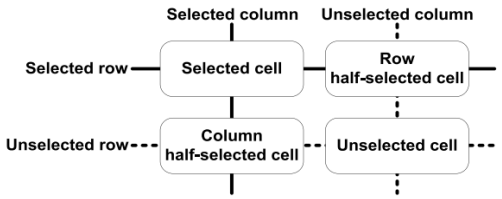

Fig. 1. Selected, half-selected, and unselected cells in a bit-interleavedSRAM array

In this bit interleaved architecture we select the SRAM cells which are used to read and write the operation. Basicakky there are two selected cells one is row half selected cell and other is column half selected cells. Row half selected cells are located at the unselected column and selected row. Columb half selected cells are located at unseleted row and selected column. Due to the selection of word line in row haf selected block the entire write operation becomes disturbed. The stability in row half selected cells the major issue is half select.by reading the stored data into one cell we can ensure the stability of the half row selected cell.suppose if we want to address the half select issue without the write back scheme then a cross point structure is proposed.

That is given as 10TSRAM cell which consists of both horizontal and verticle WLs to access the storage nodes. Now in write operation these two are selcted as one cell such that the half select issue eliminates. But the main disadvantage of tihs technologyis it occupies large area to overcome this problem another technology is introduced that is average 8T SRAM cells which is at 130nm technology. Compared to the previous technology ,

this technologyis very appropriate. But this technology also have some disadvantages that is read delay to overcome this proposed technolgy is used. In this we are going to discuss about the proposed SRAM ARCHITECTURE which oversees the delay in previous technology.

The proposed differential architecture resolves the half select issues without the need of writeback scheme. In this we use local bit line to enable the smaller delay which is obtained in circuits. At last in this paper we discuss about the SRAM technology , proposed SRAM teachnolgythat is differential SRAM technology. In this technolgy it performs both read and write operation.

II. AVERAGE-8T SRAM ARCHITECTURE

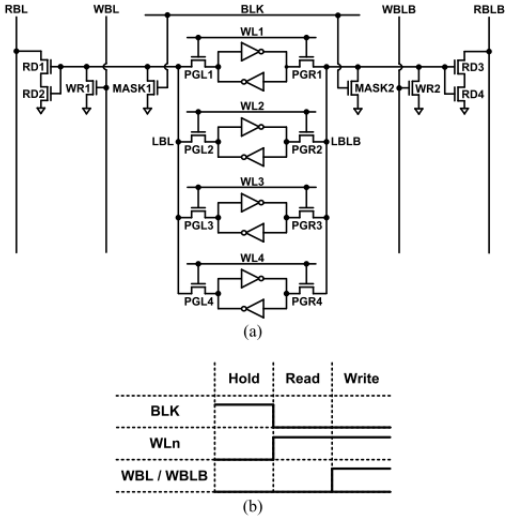

Fig. 2. (a) Average-8T SRAM architecture and (b) its operational waveform

The above figure (2) shows the architecture of average 8T SRAM. In this it consists of a bolck which stores four bits. This four bits consists of four pairs of cross coupled inverters, pass gate transistors, block mask transistors and write access transistors. In this a nmos structure is used as read buffer to reduce the leakage of BL. In this there are two block select signals one is BLK and another one is WL. The both BLK and WLs are row based signals and column based signals are BLs and RBLs. In the condition of hold state the WLs are at 0v, so supply voltage is discharged at LBL and coming to RBLs it is also set at 0v bot it charges at vdd.

To turn off the block mask transistors in read operation a block Is selected that is BLK.One selected block of BLK is at0v and another selected block is at constant. Coming to the pass gate transistors to turn this we use the WL. To store the data we selected a cell which transfers data from LBLs to pass gate transistors. In the same way to turn off the block mask transistors we select the column half selected cell. In this column half selected blocks are located at unselected rows. Coming to this architecture number of interconnections are there and this architecture is veryeffecient. We use buffers to perform the operation of both read and write. So the entire opeartion works under three conditions one is at hold and second one is read operation condition and at last third ones write operation. The main draw back this SRAM architecture is read delay and read stability. To overcome tis problems another proposed structures are proposed. That is differential SRAM architecture whete the both read and write operations. The entire process is explained in detailed manner.

III. PROPOSED DIFFERENTIAL SRAM ARCHITECTURE

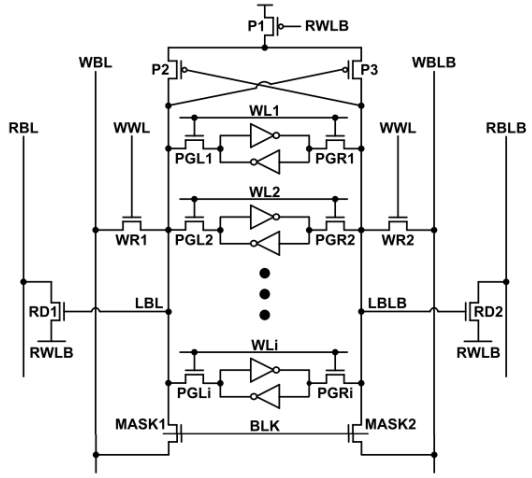

Fig. 3. Proposed SRAM architecture that stores i bits in one block

The above figure (3) shows the architecture of proposed Differential SRAM. The main advantage compared to other is that it stores multiple bits at a time in one block. Depending upon the number of bits the minimum operating voltage and area per bit vale is set. Basically this proposed architecture consists of four pairs of cross coupled inverters, block mask transistors, pass gate transistors, write access transistors, read buffers, head switch and cross coupled pMOSs. The both head switch and cross

coupled pMOSs are the special blocks of the proposed SRAM ARCHITECTURE. In this we will discuss about read and write operations in detailed manner. The entire operation in this proposed SRAM ARCHITECTURE depends on the two signals they are row based signals and column based signals. The row based signals are given as WLs (WL1~4), the block select signal (BLK), and thread WL (RWLB). Now coming to the column based signals are the writeWL (WWL), write BLs (WBL and WBLB), and read BLs(RBL and RBLB). The entire read and write operations of proposed differential architecture are shown below.

A. Read Operation

The below figure 4 (a) shows the read operation architecture of SRAM. In this read operation there are two phases; one phase is connected to the two selected blocks. One selected block of BLK is at 0v and another selected block is at constant. Depending upon the value of stored data the LBL is connected to the storage node 1. Here there is a voltage drop from pass gate transistors and the value of LBL is very low. In this the read operation is similar to the average 8T SRAM architectures. This is about first phase coming to the second phase it starts from the falling of RWLB.The value of RWLB discharges the feedback of cross coupled pMOSs. So the value of positive feedback increases the cross coupled pMOSs then value of vdd also increases. Here the WL voltage is used to enhance the stability of read and read delay. This proposed SRAM architecture eliminates the tradeoff between this two read stability and read delay. This is about the WL voltage coming to the suppressed voltage WL; this is used to enhance the read stability as well as full swing LBL which minimizes the value of read delay.

In this proposed SRAM architecture consists of single nMOS which used to buffer the read operation to increase the read current. In this buffer foot is used to reduce the leakage of RBL. In this the column half selected block is in hold state but it is not used in average 8T SRAM architecture. Coming to figure 4 (b) it consists of two selected blocks one is BLK and another one is WL. Now in this WBL is connected to the storage node 1 and it consists of 0v and the value of WLincreases when the value of BLK is reduced. So there should be time overhead at RWLB.

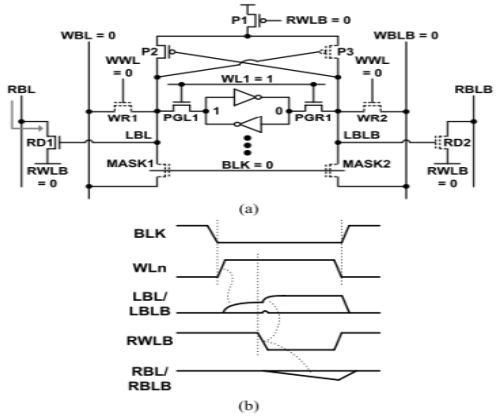

Fig. 4. (a) Read operation and (b) read operational waveform of proposed RAM architecture.

B. Write operation

The below figure 5(a) shows the architecture of write operation SRAM. In this there are two selected blocks; one selected block is BLK consists of 0v and coming to another selected block that is WL remains constant. Coming to the selected block WWL is at input vdd because of it the transistors are in on position and WBLs are set at certain voltage level. Basically write operation consists of storage nodes and these storage nodes are connected to the WBLs. These WBLs consists of both pass gate transistors and write access transistors. From this when we compared with average 8T-SRAM architecture the proposed structure is differential and single ended.

Coming to the figure5 (b) it is row half selected block. This operation is similar to the read operation but the value of RLWB is high. In this the storage nodes also connected to the read operation block. Compared to the average 8T SRAM architecture in this figure the entire operation is same as read operation. In this row half selected block operation it eliminates the RBL discharge and there is large amount of dynamic power. This is about row half selected block coming to figure 5 (c), it is about half column selected block. In this block mask transistors are connected to vss. In the dc current flows from high WBL to the vss from write access and mask transistors. In this write operation the both BLK and WL are high and it consists of large amount of static power. This write operation eliminates the sources of block mask transistors to WBL.

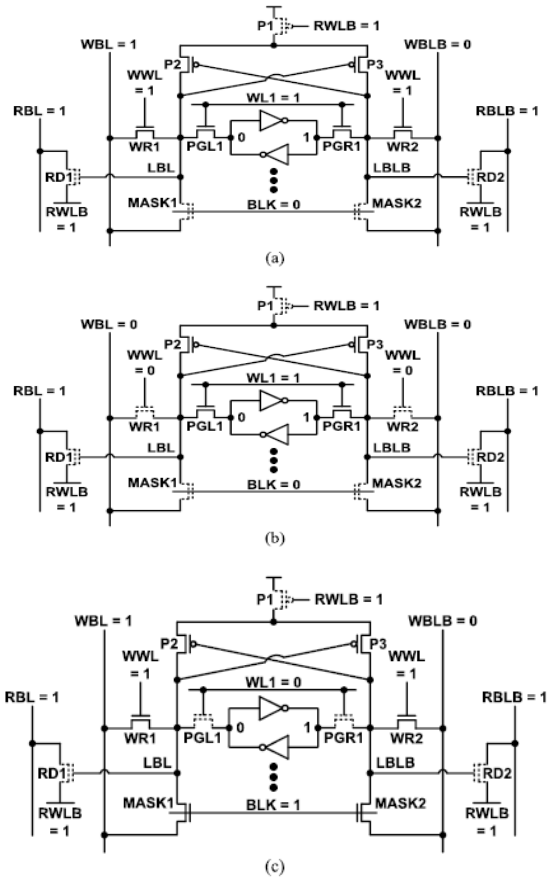

Fig. 5. (a) Selected, (b) row half-selected, and (c) column half-selected blocks of proposed SRAM architecture during write operation

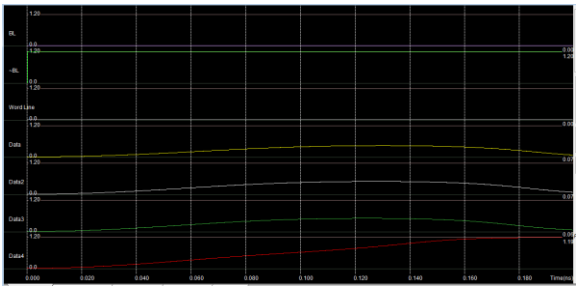

Fig. 6. Result of SRAM

IV. CONCLUSION

Basically in average 8T SRAM architecture there is no need of write back scheme in bit interleaving. This architecture depends on the advanced technology that is 22nm FinFET technology. In this we us as full swing LBL which provides tradeoff between read delay and read stability. But in this the gate of read buffer does not passes through the vdd. In this the write operation of RBLs the unselected columns gets discharged. Because of this there is consumption in large amount of dynamic power. This is about the average 8T SRAM architecture coming to the proposed SRAM ARCHITECTURE eliminates the tradeoff between the both read delay and read stability. By using cross coupled pMOSs we can get a full swing which moves from the vdd. To enhance the read stability we use suppressed WL circuit. As discussed earlier that we use nMOSs structure for the purpose of read buffer to increase the read delay. At last we can say that the in proposed SRAM ARCHITECTURE we use advanced technology that is 22nm FinFET technology. This technology produces small read delay and consumes less energy.

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