# Fuzzy logic controller based DC-Link Voltage Self-Balance Method for Multilevel Converter with less Number of Voltage Sensors

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***Abstract*- In many inverters, Voltage balance of dc- link capacitors is very important for applications of a cascade multilevel converter or a modular multilevel converter. In this paper, a novel diode-clamped modular multilevel converter (DCM2 C) topology is proposed and a power feedback control method is developed with fuzzy logic controller. With the developed control strategy, the proposed diode-clamped circuit becomes controllable closed loop which enables the capacitor voltages to be clamped by low power rating clamping diodes. The proposed topology and control strategy has quicker response with transient state error reduction and requires much fewer voltage sensors than the normally used traditional method of multilevel inverters as diode clamped inverters; therefore, the system performance improvement and cost reduction are expected. Based on the proposed DCM2 C, a novel N +1-level cascade multilevel topology is proposed for a cascade active power filter (CS -APF). The Proposed fuzzy logic controller is implemented to get study state response at dc voltage capacitors, therefore to get balanced load outputs. The simulation results from the CS -APF have demonstrated and verified the effectiveness of the proposed novel topology and control method.**

***Index Terms*- Capacitor voltage balance, cascade active power filter (CS -APF), diode-clamped modular multilevel converter (DCM2 C), minimum number of voltage sensors, fuzzy logic controller.**

## I. INTRODUCTION

Now a day's power converters are playing key role in power system applications. Power electronic devices with less losses and useful for medium and high power applications causes to grow, for instance, an active power filter (APF) which is an ideal choice for power conditioning [1]–[3]. A high switching frequency is normally required for such electronic converters to achieve good performance, such as fast response, good filtering, and low harmonics; however, the high switching frequency may limit the capacity of a normal two-level converter due to the power loss.

A multiple converter configuration may be an effective solution for high-power medium-voltage applications [4]–[7], but a bulky transformer is usually required. Recently, the topologies of multilevel converter have become popular in medium-voltage applications, because of its features of simple structure, modularity, and transformer-less. In particular, the multi modular converter based on half- bridge or full-bridge topology is a good solution for medium-/high-voltage applications, including STATCOM, APF, and HVDC. However, the dc-link capacitors are floating in either a full-bridge cascade converter or a half-bridge cascade converter. Due to the difference of parasitic parameters between cells, the non ideal drive pulses, and so on, the dc-link capacitor voltages may become unbalanced if a specifically de-signed control method is not in place. Some capacitor voltage balance control algorithms are studied. These methods may be classified into the following categories:

1. Switching patterns rotated (SPR) methods;
2. Fundamental voltage vector regulation (FVVR) methods; and
3. Direct duty cycle (DDC) control methods.

By adding an auxiliary circuit to each cell for exchanging energy between cells, capacitor voltage balance can also be realized. However, such an auxiliary circuit usually requires an extra inverter and a control circuit, maybe also a transformer if isolation

is required, which will significantly Increase the circuit complexity and cost.

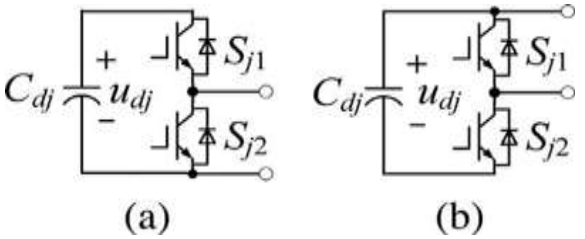


Fig.1.Two basic topologies of a half-bridge cell

A novel simple diode-clamped modular multilevel converter (DCM2C) topology is proposed in this paper. It is based on the cascade connection of half-bridge cell converters. Via adding a clamping diode to each cell's dc bus, the capacitor's voltage of one cell could be clamped by the two neighboring cells when the circuit works. At the same time, an energy feedback cir-cuit is used for connecting the top and bottom cells, so that a closed loop clamping circuit is formed. In this topology, only the top and bottom cells need the voltage sensors, which significantly reduce the required number of sensors. Furthermore, a performance enhancing control algorithm is implemented in the controller to ensure a quick response by the rectifier. If the dc voltage of cell N is lower than that of cell 1, energy will be transmitted from Cd1 to CdN via the feedback circuit. Then, udN will rise and ud1 will drop, so ud 1 and udN will be equalized by the feedback circuit. Therefore, a closed voltage clamping circuit is realized.

Considering the leakage inductance of Tac and the voltage drop of the switches, wT should be a little larger than 1, and the output power of the auxiliary circuit can be controlled by adjusting the pulse width modulation (PWM) duty cycle of cell 1.

The AFBI needs four active switches, while an auxiliary half bridge inverter (AHBI) needs only two active switches as shown in Fig. 2(b), and the winding turning ratio of the transformer is 1: wT = 1: 2 (Similarly, wT > 2 in practical application). Besides, a capacitor Cac is connected to the primary winding of Tac in series to block the dc component. DC-link voltage unbalance is mainly caused by the loss difference between cells and the non ideal drive pulses, and such unbalance could be removed with much lower power comparing with that of the main circuit. Then, another feedback topology with a simpler structure is proposed, as shown in Fig. 2(c).

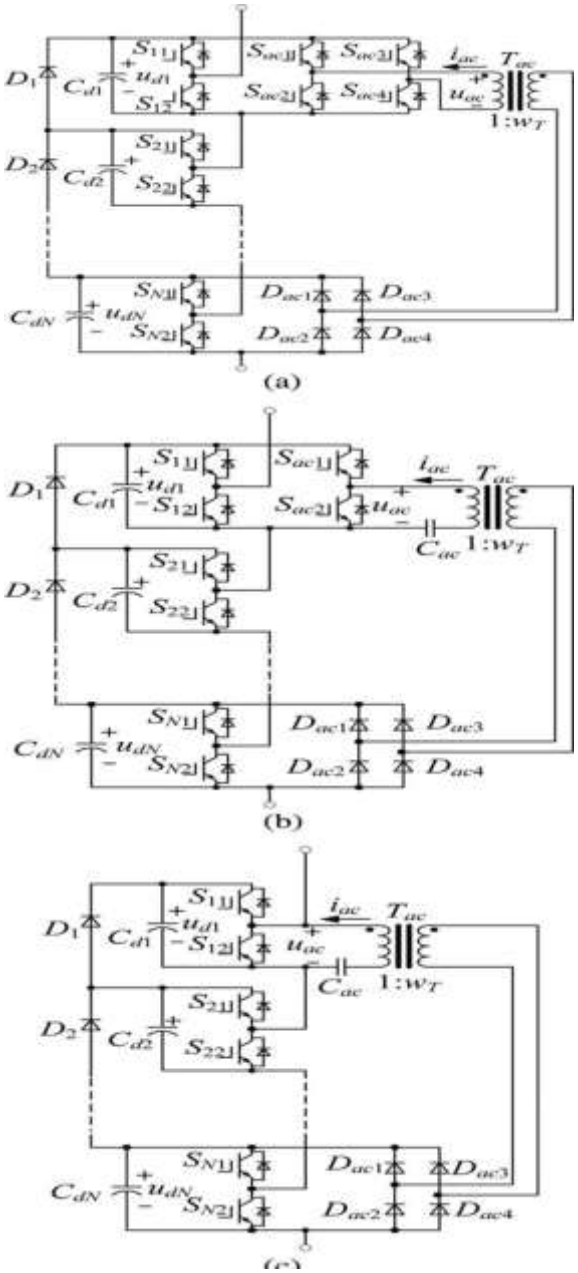


Fig. 2.Three kinds of feedback topologies. (a) Circuit based on AFBI (UCT).(b) Circuit based on AHBI (UCT). (c) Circuit based on SHI (UCT)

TABLE I SUMMARY OF THREE AUXILIARY CIRCUITS

| Type | Advantages | Disadvantages |
|---|---|---|
| AFBI | Independent of the main circuit<br>Flexible control | Switch number is high<br>Require additional control circuit. |
| AHBI | Fewer active switches than AFBI<br>Independent of the main circuit<br>Flexible control | Require additional control circuit. |
| SHI | Simple structure<br>No extra active switches<br>No extra control circuit<br>Higher efficiency | Not independent of the main circuit |

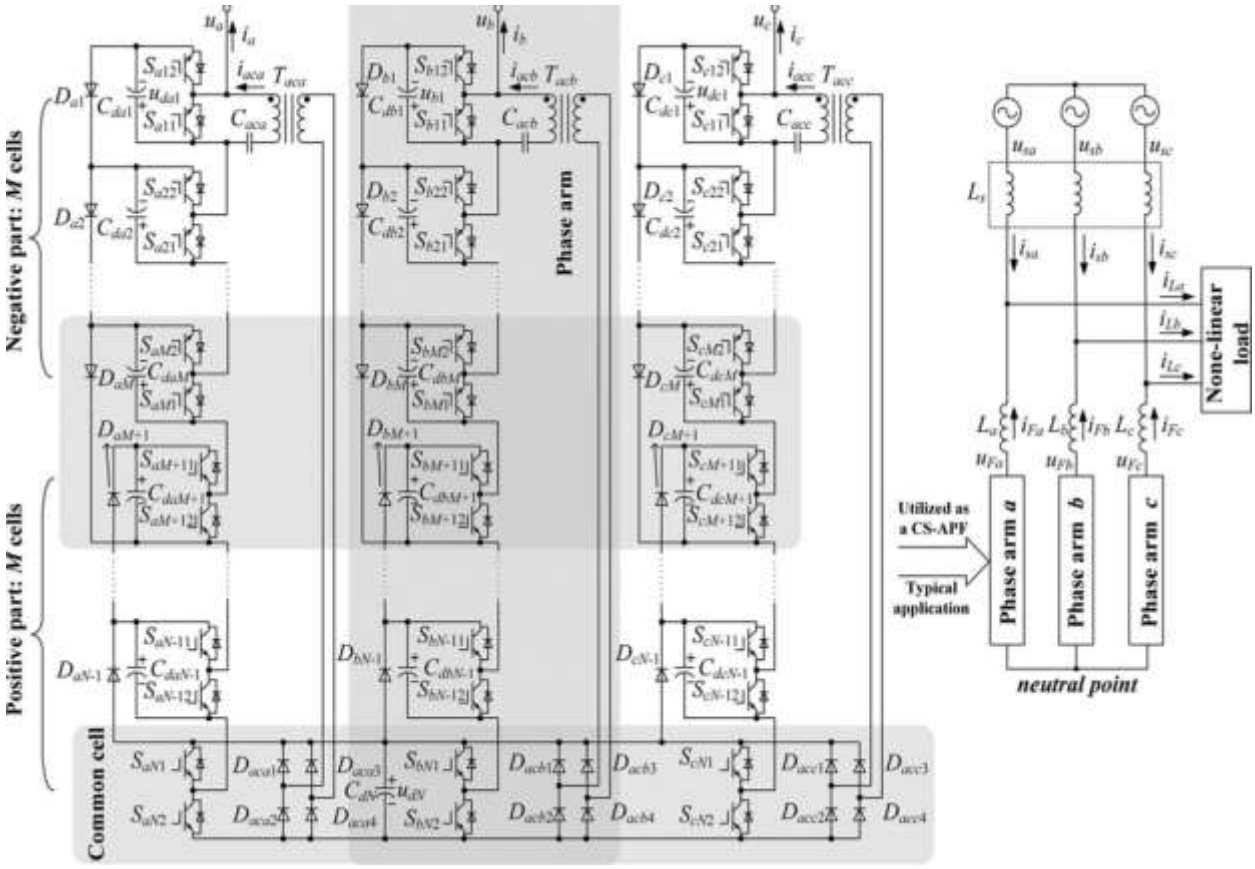


Fig.3. Topology of a three-phase converter based on DCM2C (N = 2M)

## II.THREE-PHASE DCM2CWITH STAR CONFIGURATION

### A. Three-phase converter topology based on dcm2c

Delta configuration and star configuration are two common choices for a cascade converter. Because the number of the cascade cells of the star configuration is smaller than that of the delta configuration for the same voltage level application, the star configuration is chosen here for discussion.

The proposed topology of a three-phase DCM2C is shown in Fig. 9.It contains three phase arms for phase a, phase b, and phase c, respectively, with the same structure. The three arms are connected to a common neutral point. The converter is directly connected to a medium voltage network via three inductors without a transformer.

2M cells are connected in series in each phase arm, and divided into two parts: the positive part and the negative part, by which the positive and negative voltages are generated, respectively. Thus, the topology is a 2M+1-level converter. The UCT is arm is connected with the feedback circuit (SHI).

The three bottom cells (or the common cell of the three used for the cells in the positive part and the DCT for the negative part; thus, the common- mode voltage at the neutral point (taking the ground or the neutral point of the network as zero potential) will be reduced for easing the insulation. The top cell of each phase phases) share a common dc bus which is also shared by the three rectifiers of the feedback circuits.

The common cell provides energy exchange channels between the three phases which is beneficial to the dc-link voltage balance among three phases and also has the merits in reduction of the required number of voltage sensors. As a result, only four dc- link voltage sensors are required, and placed at the top three cells and the bottom cell for the system control.

### B. Efficiency analysis of the proposed topology

There is no auxiliary circuit in the traditional cascade multilevel topologies and the capacitor voltage balance control is done by the software, while the proposed topology, DCM2C, is equipped with clamping diodes and there will be current flowing through them. Thus, the efficiency of a DCM2C is a little lower than that of the traditional topology.

In fact, the current flowing through the clamping diodes and the auxiliary circuit is much lower than rated current of main circuit. According to the analysis in Section II, the capacitor voltage unbalance is caused by the loss difference and non ideal drive signals, and so on; thus, power for equalizing the capacitors between two cells is usually not higher than 5% of Pcell. Then, if total power of clamping circuit Pe is 5% of the system's rated power Pr and the efficiency of clamping circuit is 90%, the loss Ploss e of clamping circuit could be calculated as follows:

In fact, the clamping circuit will not run at the maximum power point all the time. Thus, the average loss of the clamping circuit will be lower than (29). Therefore, the clamping circuit has little influence on the system efficiency in the steady state.

C. Summary of the proposed topology

Generally speaking, the proposed topology has the merits in the following aspects:

1. the capacitor voltages of the dc link are self-balanced, and the capacitor voltage balance control is completely independent from the voltage and current of the main circuit;
2. Only four dc-link voltage sensors are required in the topology. The measurement and control circuit is simple;
3. the auxiliary circuit control algorithm is simple and takes up little time for calculation and the complex control algorithm can be implemented with this topology for high performance;
4. The power rating of clamping diodes and feedback circuit is very low. Thus, it is low cost;
5. Since the power rating of auxiliary circuit is low, it has little influence on the system efficiency.

## III. CONTROL OF A DCM2C AS A CS-APF

Applied as a CS-APF, the proposed topology based on DCM2C (see Fig. 4) is discussed in the following aspects in this section:

1. Harmonic detection and compensation control;
2. Current loop control;
3. DC-link voltage control: phase arm dc-link voltage control and auxiliary clamping circuit control;
4. Modulation method.

Since the capacitor voltage balance is done by an auxiliary circuit, the digital controller has more time to realize a complex control algorithm, as Fig. 10 shows. The harmonics suppression control includes a load current feed-forward control and a source current feedback control [32].

In the feedback control loop, a selective harmonic detection method based on bandpass filters is used to improve the control precision with little influence on the stability.

The source currents (isa, isb, isc) are transformed into αβ coordinates. i∗ shα and i∗ shβ are the harmonic components of the source current. The controllers for the feedback control are two P regulators. C32 and C23 are the Clarke transformation and the inverse Clarke transformation

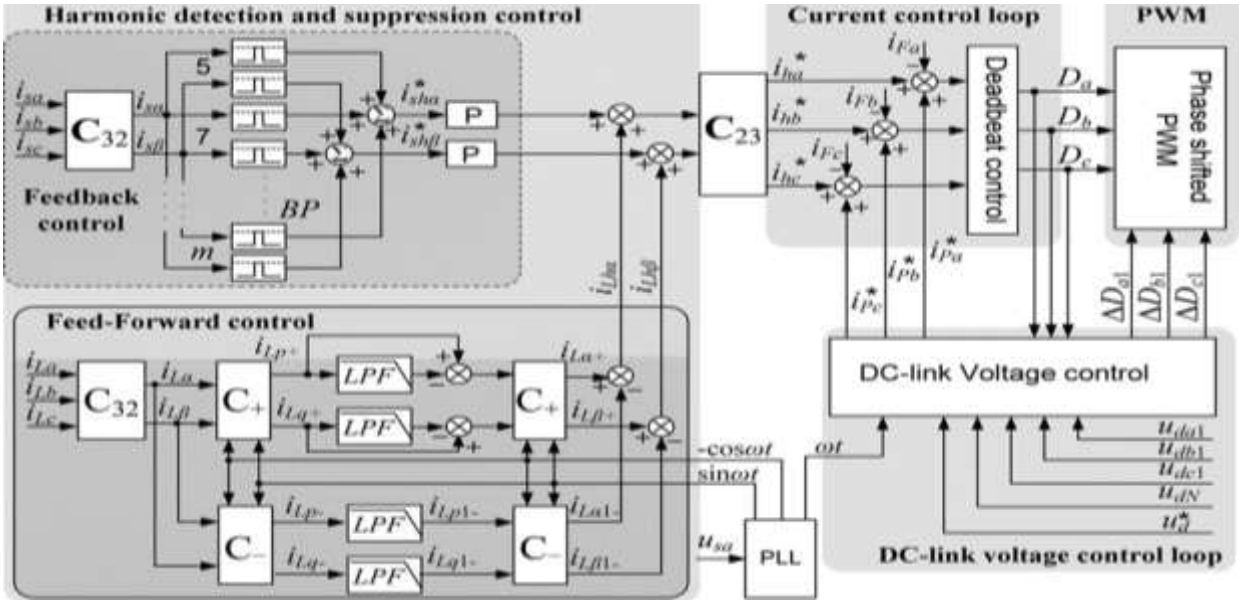

Fig.4. Control scheme of a CS-APF based on DCM2C

The harmonic detection method for feed- forward control is based on the famous instantaneous reactive power theory for an improved dynamic response. The load currents (isa, isb, isc) are transformed into αβ coordinates (iL α, iLβ). iLα and iLβ are then transformed into the positive-sequence pq coordinates (iLp+, iLq+) where the positive-sequence fundamental components

## IV.IMPLEMENTATION OF FUZZYLOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as;

1. Seven fuzzy sets for each input and output.
2. Triangular membership functions for simplicity.
3. Fuzzification using continuous universe of discourse.
4. Implication using Mamdani"s„ min" operator.
5. Defuzzification using the „height" method.

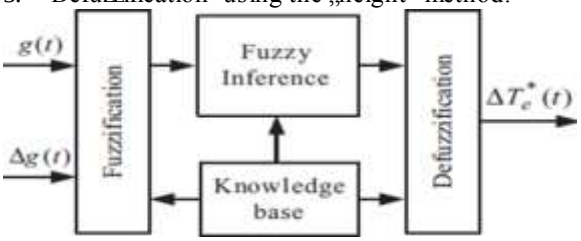


Fig.5.fuzzy Logic Controller

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

A large value of error E indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible.

One the other hand, small value of the error E indicates that the system is near to balanced state. Overshoot plays an important role in the system stability. Less over shoot is required for system stability and in restraining oscillations. C in (12) plays an important role, while the role of E is diminished. The optimization is done by α. The set of FC rules is given in Table III.

TABLE II. FUZZY RULES

| e / Δe | NB | NM | NS | ZE | PS | PM | PB |
|---|---|---|---|---|---|---|---|
| NB | NB | NB | NB | NB | NM | NS | ZE |
| NM | NB | NB | NB | NM | NS | ZE | PS |
| NS | NB | NB | NM | NS | ZE | PS | PM |
| ZE | NB | NM | NS | ZE | PS | PM | PB |
| PS | NM | NS | ZE | PS | PM | PB | PB |
| PM | NS | ZE | PS | PM | PB | PB | PB |
| PB | ZE | PS | PM | PB | PB | PB | PB |

## V. SIMULATION RESULTS

### A. Simulation Study with PI Controller

A simulation model of a seven-level CS- APF based on DCM2C has been designed. The topology is the same as the one shown, and the system control is presented

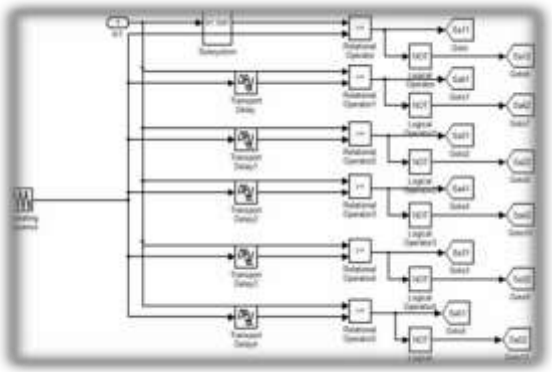

Fig.6.pulse generation for inverter switch

A resistor is connected to each cell's capacitor in parallel, and the differences of power loss between cells are simulated with different values of the resistors. Fig. 7 shows the simulation results of the proposed seven level CS-APF. The sequence of the waveforms is (from top to bottom) isa, iLa, and iF a. The distorted source current is well corrected by the CS-APF.

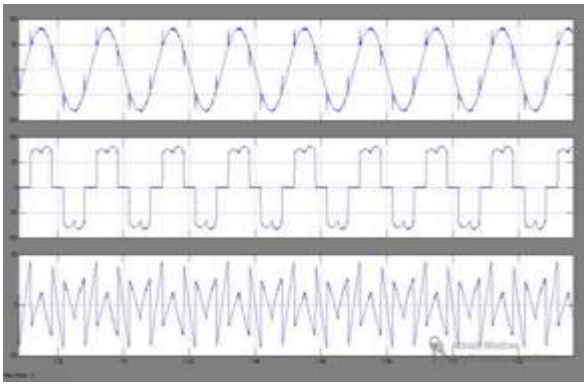

Fig.7. Simulation waveforms of isa , iLa , and iF a

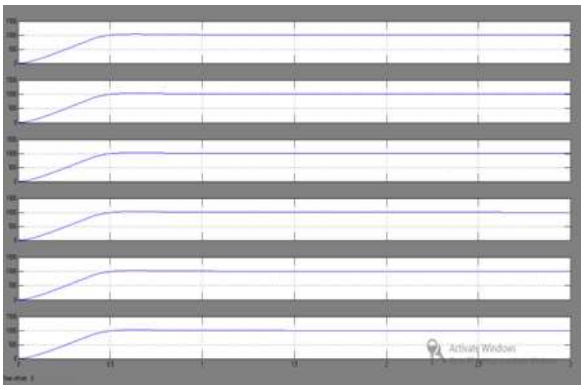

Fig.8. DC-link voltages of CS-APF (phase a) with the clamping circuit in operation.

The dc-link voltages of a seven-level CS- APF based on DCM2C are presented in Fig. 9(phase a). The capacitor voltages are well balanced by the clamping circuit, and the voltage differences are not higher than 10 V. Besides, the voltage ripples of CdN are very low for the common cell shared by the three phases

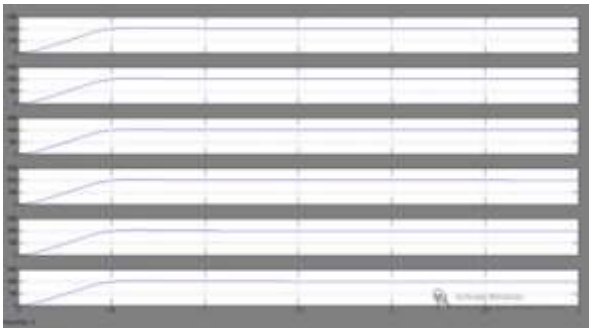

Fig.9. DC-link voltages of CS-APF based on DCM2C with energy feedback circuit turned OFF.

Fig.9 shows the simulation results of the dc-link capacitor voltages of the proposed seven- level CS-APF with the energy feedback circuit turned OFF. The capacitor voltages become unbalanced. However, with the clamping diodes working, the relationship of the capacitor voltages is uda1 > uda2 > uda3 > uda4 = uda5 > udN .

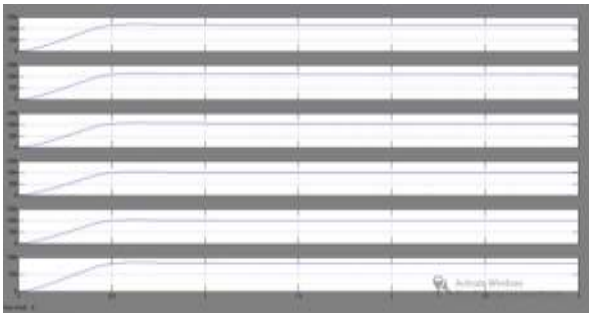

Fig.10. DC-link voltage of a CS-APF based on basic half-bridge inverter.

Fig. 10 shows the simulation results of a seven-level CSAPF based on the basic half-bridge inverter. With no voltage balance control, the dc-link capacitor voltages gradually become unbalanced. Unlike that in the system based on DCM2C, the relationship of the voltages is uda3 > uda5≈uda1 > uda2 > uda4 > udN . It is similar to the relationship of the resistance in Table IV: Ra3 > Ra1 > Ra5 > Ra2 > Ra4 > RaN

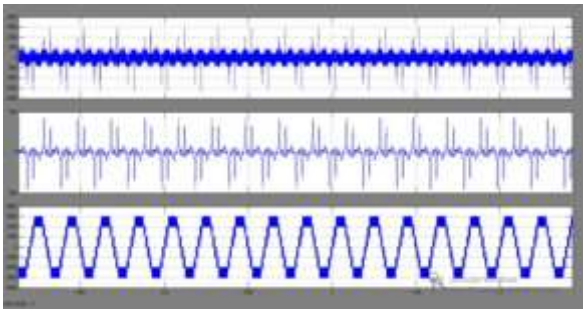

Fig.11. Common-mode voltage of the neutral point of the proposed CS-APF.

The common-mode voltage of the neutral point of a seven level CS-APF based on DCM2C is shown in Fig. 11. The sequence of the waveforms is (from top to bottom) un, u_ n , and uF a. un is the voltage between the negative pole of CdN and the neutral point of the power source. It is much lower than the source voltage. u_ n is the voltage filtered from un by a low-pass filter with the cutoff frequency of 1 kHz. u_n is lower than 200 V. uF a is the voltage of phase arm a of the CS-APF, and is seven- level voltage.

B. Simulation network with fuzzy logic controller

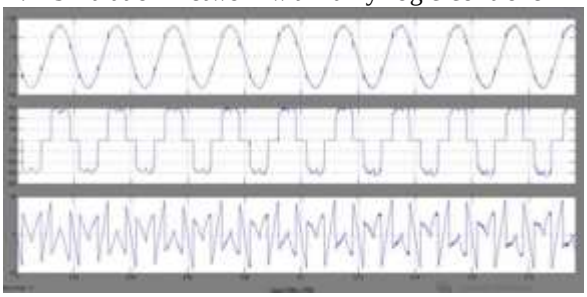

Fig.12. Simulation waveforms of isa , iLa , and iF a

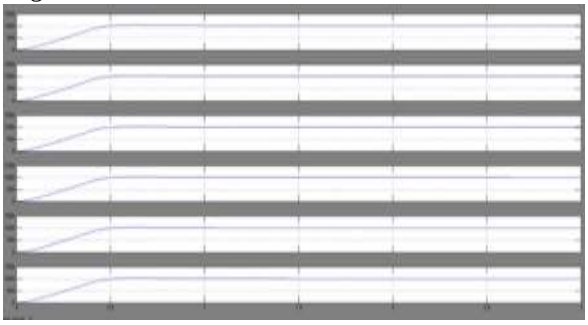

Fig. 13. DC-link voltages of CS-APF (phase a) with the clamping circuit in operation

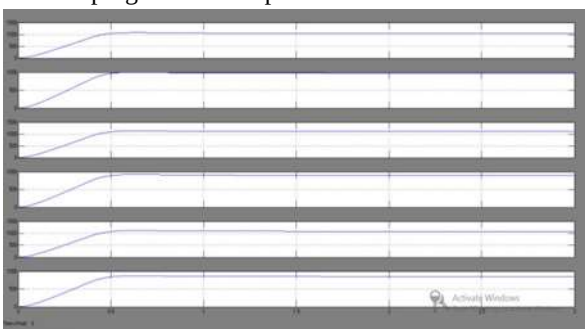

Fig.14. DC-link voltages of CS-APF based on DCM2C with the energy feedback circuit turned OFF

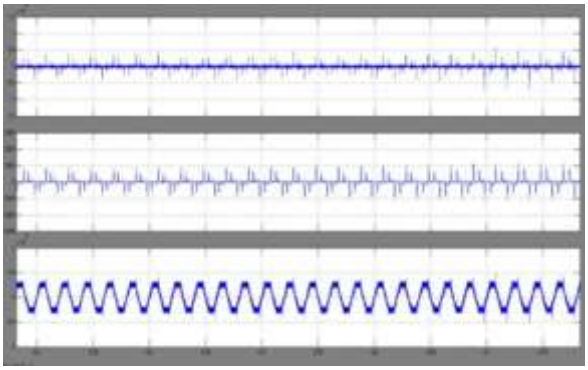

Fig.15.Common-mode voltage of the neutral point of the proposed CS-APF

## VI. CONCLUSION

A novel topology of a DCM2C is proposed in this paper using fuzzy logic controller. The topology is proved to be a suitable solution for high- voltage and high-power application instead of using pi controller. Voltage balance for all dc-link capacitors is realized with a proposed simple feedback auxiliary circuit. The number of dc-link voltage sensors could be decreased significantly, and also the transient time interval and study state time interval gets reduced which reduces control complexity and system cost. Three kinds of auxiliary circuits are resented and analyzed in this paper.

The novel topology of a three-phase DCM2C with the auxiliary circuits (SHI) is applied as a CS- APF, and the system control algorithm and specific mathematical model are presented. With only four voltage sensors at the dc-link side, the dc-link voltages are well balanced. Furthermore, the complexity of the system control algorithm does not increase with the number of cells increasing. The system can operate under normal condition even only one phase auxiliary circuit is in operation. So, the reliability of dc-link voltage balance is significantly enhanced. With simple topology, perfect clamping performance, and very small number of voltage sensors, a DCM2C is a perfect solution for medium-/high-voltage applications. It can be useful in many applications, such as HVDC, STATCOM, etc.

## REFERENCES


[1] H. Akagi, "New trends in active filters for power conditioning," IEEE Trans. Ind. Appl., vol. 32, no. 6, pp. 1312–1322, Nov.–Dec. 1996.

[2] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active power filters for power quality improvements," IEEE Trans. Ind. Electron., vol. 46, no. 5, pp. 960–971, Oct. 1999.

[3] H. Akagi, "Active harmonic filters," in Proc. IEEE, Dec.2005, vol. 93, no. 12, pp. 2128–2141.

[4] J. Ju, D. Xu, M. Chen, J. Xu, B. Shen, and F. Zhang, "Control strategy of multi-modular active power filter system," in Proc. IEEE Appl. Power Electron. Conf, Mar.2007, pp. 686–691.

[5] T. Lee and P. Cheng, "Design of a new cooperative harmonic filtering strategy for the distributed generation systems," in Proc. IEEE 40th Ind.Appl. Soc. Annu. Meet. Ind. Appl. Conf., Oct.2005, pp. 549–556.

[6] P. Cheng and Z. Lee, "Distributed active filter systems (DAFS): A new approach to power system harmonics," in presented at the IEEE 39th Ind. Appl. Soc. Annu. Meet. Ind. Appl. Conf., Seattle, WA, Oct.2004.

[7] M. Rastogi, P. W. Hammond, and S. R. Simms, "Multi-level active filter for medium voltage applications," in Proc. Power Electron. Drives Syst., Nov. 2005, pp. 1508–1513.

[8] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series- connected symmetrical and asymmetrical diodeclamped H-bridge cells," IEEE Trans. Power Electron., vol. 26, no. 1, pp. 51–65, Jan. 2011.

[9] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J.-K. Lim, M. Bakowski, L. Angquist, and N. Lee, "High-power modular multilevel converters with SiC JFETs," IEEE

Trans. Power Electron., vol. 27, no. 1, pp. 28–36, Jan. 2012.

[10] H. P. Mohammadi and M. T. Bina, "A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1534–1545, May 2011.

[11] F. Z. Peng and J. Wang, "A universal STATCOM with delta-connected cascade multilevel inverter," in Proc. 35th Annu. IEEE Power Electron. Spec. Conf., Jun. 2004, pp. 3529–3533.

[12] R. E. Betz and T. J. Summers, "Using a cascaded H-bridge STATCOM for rebalancing unbalanced voltages," in Proc. 7th Int. Conf. Power Electron., Oct. 2007, pp. 1219–1224.

[13] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," IEEE Trans. Ind. Electron., vol. 43, no. 4, pp. 1041–1049, Jul.– Aug. 2007.

[14] Q. Song and W. Liu, "Control of a cascade STATCOM with star configuration under unbalanced conditions," IEEE Trans. Power Electron. vol. 24, no. 1, pp. 45–58, Jan. 2009.

[15] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2008, pp. 174–179.