A Novel Fault Tolerant Topology of Active Neutral Point Clamped Inverter

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***Abstract*- Amongst all power electronic devices, semiconductor switches are most vulnerable to failure. On the other hand, MLIs incorporate a high device count which combined with their vulnerability characteristic lead to a high probability of failure leading to mal-operation of MLI. There are two types of fault mainly occurring in semiconductor switches, open circuit failure and short circuit failure. A short circuit failure results in shoot through condition through DC voltage source or capacitor, which causes a huge surge current to flow through the remaining healthy part of the inverter, thereby decreasing the reliability of the inverter. This condition can be avoided by connecting the fuses to the legs of the inverter, which results in converting a short circuit failure into an open circuit fault. Therefore, it is necessary to bypass faulty switch in power semiconductor switches to preserve the health of the inverter and avoid total system shutdown. Thus, only the open circuit fault tolerant operation has been studied in the entire length of the paper of the proposed topology. A unique position of redundant switches helps to achieve the fault tolerant operation for the proposed topology.**

Index terms- Multilevel Inverter, Active Neutral Point Clamped, Fault Tolerant

I. INTRODUCTION

Due to advancement in the power semiconductor devices, converters have been extending their range of use in many industrial sectors. Particularly, dc/ac converters are gaining more attention due to significant advantages such as reduction in the energy consumption, increased efficiency of system, better quality of product, reduced maintenance, and many more. In case of the medium voltage applications with grid, a conventional two level inverter suffers from different drawbacks [1-3]. To overcome this drawbacks a multilevel power converter structure has been introduced as an alternative for high power and medium voltage applications such as High Voltage DC Transmission System (HVDC), static compensators (STATCOM), electric and hybrid electric vehicles, uninterruptable power supplies (UPS) laminators etc. Multilevel converter provides a good solution between cost and performance when compared to conventional two level converters. These converters can be employed for high power as well as low power applications in combination with renewable energy sources such as photovoltaic, wind, and fuel cells. These sources can be easily operated in connection with multilevel converters for a high power application. Since the origination of multilevel converters, they have been utilized in traction, both in locomotives and track-side static converters [4]. Recently multilevel converters are heavily influenced by applications such as power system converters to achieve VAR compensation and stability improvement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most recently they have been employed for medium voltage induction motor, variable speed drives [8]. Multilevel converters are mostly employed for applications such as industrial medium-voltage motor drives [3- 9], grid connected renewable energy systems [10], Flexible AC Transmission System (FACTS) [11], and traction drive systems [12]. These application demands the converters performance in terms of high voltage and low power requirement. Due to this reason, high-voltage and large-power inverters have been developed for two-level output which employs series combination of switching power devices such as Gate Turn Off thyristors (GTOs), Integrated Gate Commutated Transistors (IGCTs), and Integrated Gate Bipolar Transistors (IGBTs).This is due to the objective to achieve higher voltage levels with series connection of switches. However, the series combination of power switches

leads to several issues [13], such as non-uniform distribution of source voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices when operating for transient and steady-state conditions. The higher blocking voltage of the switches leads to the higher cost of the device and increased switching also adds up the extra losses. In order to solve the aforementioned issues, considerable amount of circuit topologies of multilevel inverter and converter have been proposed in literature. The load voltage in case of the multilevel inverter is attained in staircase pattern from combination of several DC voltage sources. The load voltage quality increases with increase in number of voltage levels. Due to this the size of output filters is reduced which decreases the cost of inverter.

In 1975, the concept of multilevel inverters has been introduced with the first proposed topology of cascaded multilevel inverter [14]. Several individual full bridge cell supplied from DC voltage sources are placed in series to attain a staircase AC voltage waveform pattern. Primarily the multilevel inverters are realized in terms of three-level load voltage waveform [15]. Based on this, many multilevel converter topologies have been designed and studied in literature [16]. In 1981, a new multilevel inverter topology named as the Neutral-Point Clamped (NPC) inverter design was proposed [17]. In 1992, capacitor-clamped (also known as flying capacitor) type topology of multilevel inverter, [18] and in year of 1996 topology of cascaded multilevel inverter was proposed [19]. Even though the cascade multilevel inverter type topology was invented previously, in the perspective of practical application it did not come into the light till the mid-1990s. This topology has several advantages in view of the applications of several motor drives and grid connection. The cascaded type topology of multilevel inverter has received significant attention due to modularity and simplicity in architecture. In [20-21], the main application of the cascade inverter for regenerative-type motor drive is studied. Recently, several novel topologies are emerging in literature due to scope of development in terms of cost and performance. This involves conventional topologies of multilevel inverters [22], combination of different conventional type topologies of multilevel inverters [23], hybrid multilevel inverters [24-25] and soft-switched multilevel inverters [26]. These multilevel inverters can be well utilized for higher voltage applications with increase in voltage levels. The equivalent switching frequency can be altered without the change in actual switching frequency, thus the ripples are reduced in load voltage and it also reduces the electromagnetic interference (EMI). The architecture of different multilevel converters can be framed in several ways. The general strategy involves the parallel or series connection of conventional converters to form the staircase waveform pattern of load voltage [27]. More complex structures are developed by adding number of converter cells inside of the main converter structure [28]. The total voltage or current rating of the topology of multilevel converter can be evaluated by summation of the rating of combination of individual switches, and so the power rating of the converter can exceed the rated voltage and current values of the individual power switches. The basic concept behind the idea of multilevel inverter is to attain high power with series combination of switches having several lower voltage dc sources to perform the conversion of power by achieving a staircase voltage waveform. The isolated DC voltage sources can be easily replaced by different alternatives such as capacitors, batteries and renewable energy sources. The operation of the power switches combine these multiple dc sources in order to attain high voltage at the output; however, the rated voltage across main power switches based upon the rating of the dc voltage sources applied across the main converter structure.

II. OPERATION OF ANPC TOPOLOGY

In fig 1, the configuration of active neutral point clamped (ANPC) topology of multilevel inverter is shown. This topology generates five level output voltage with the switching scheme shown in table 1. The architecture of this topology comprises of two individual legs of ANPC topology which are connected in parallel. Each leg of ANPC topology generates three level output voltage. The topology comprises of 12 power switches, 2 capacitors to divide the input DC voltage. The topology of ANPC provides a considerable trade- off between the inverter cost and performance and thus, it is found to be gaining more attention. This topology eliminates

the requirement of bidirectional switches which further reduces the cost of extra gate driver circuits and heat sinks.

The switching scheme considered for the operation of this topology is summarized in table-1 as shown below. This switching scheme consists of various switching sequences required to generate corresponding voltage levels. The effect on the state of the capacitors C1 and C2 are also mentioned along with the switching path to generate each voltage level, while the generation of each voltage level. This switching scheme takes the flyback effect in consideration while generation of each voltage level. The flyback effect is defined by the spikes in the output voltage waveform across a reactive load caused due to sudden reduction or interruption in the supply current. When the supply current abruptly changes its magnitude i.e. decreases enormously, it leads to the flyback effect which can be seen in the waveform of output voltage. It is of great importance to reduce this effect as this effect may leads in the decreased quality of output voltage waveform by increasing the harmonic content.

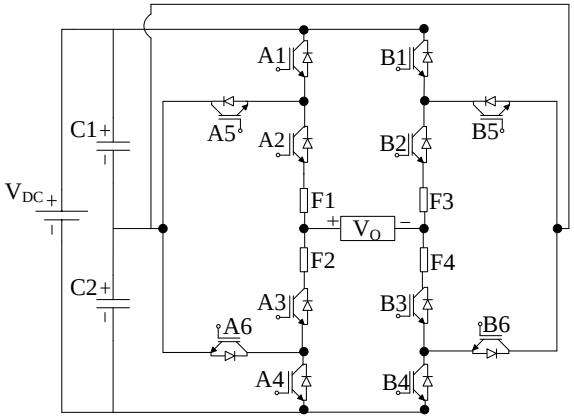

Fig. 1 Structure of Active neutral point clamped (ANPC) Topology of multilevel inverter

Table-1 Switching scheme table for 5 level ANPC converter

Output voltage level	Sequence	Switching scheme	Effect on capacitor C1	Effect on capacitor C2
V_{DC}	Seq 1	A1, A2, B3, B4	No effect	No effect
$V_{DC/2}$	Seq 2	A1, A2, B3, B6	Discharge	Charge
	Seq 3	A2, A5, B3, B4	Charge	Discharge
	Seq 4	A1, A2, B1, B2	No effect	No effect
0	Seq 5	A3, A4, B3, B4	No effect	No effect
	Seq 6	A2, A5, B2, B5	No effect	No effect
	Seq 7	A2, A5, B3, B6	No effect	No effect
	Seq 8	A3, A6, B3, B6	No effect	No effect
	Seq 9	A3, A6, B2, B5	No effect	No effect
$-V_{DC}/2$	Seq 10	A2, A5, B1, B2	Discharge	Charge
	Seq 11	A3, A4, B2, B5	Charge	Discharge
$-V_{DC}$	Seq 12	A3, A4, B1, B2	No effect	No effect

II. MODULATION STRATEGY

The implementation of appropriate modulation strategy is important in order to minimize the total harmonic distortion (THD) and improve the power quality of the output voltage waveform. The gate pulses control the switching ON and OFF state of an IGBT device. These pulses are primarily fed to the input of gate driver circuit of power semiconductor switches. A gate driver is a power amplifier that receives a low-power input with the help of a controller IC and generates a high-current drive input for the gating of an IGBT switch. The gate pulses for the operation of five levels ANPC topology are obtained by the strategy of level shift pulse width modulation (LS-PWM). This strategy is implemented by employing multiple carrier waves. These carrier waves are triangular in nature which can be used to alter both of the falling and rising edge of the pulses. This helps to improve the harmonic spectrum of the output voltage. In this LS-PWM, the sinusoidal reference signal of fundamental frequency is compared with the high frequency carrier wave which generates the respective pulses. The ratio of peak amplitude of these two waves decides the modulation index (Ma). The mathematical formula of modulation index (Ma) for N level MLI is given as:

$$Ma = Vref / Vcar \quad \ldots\ldots\ldots (1)$$

Where, Vref indicates the maximum amplitude of sinusoidal reference signal and Vcar is showing the peak to peak amplitude of triangular carrier waves. The variation of modulation index takes place in the range of 0 to 1 for the linear operation of multilevel inverter. The amplitude of output voltage is increased

with the increase in the value of modulation index. Total harmonic distortion (THD) of phase-shifted modulation is considerably higher than level-shifted modulation. Therefore only level-shifted modulation is considered. An n-level CHB inverter which employs level-shifted multicarrier modulation scheme demands (n-1) triangular carriers, all having the same frequency and amplitude. The (n-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous.

III. HEALTHY OPERATION

The healthy operation of ANPC topology of MLI is studied in the MATLAB/Simulink. The simulation is carried out for the R-L type of load having the values of R= 20 ohm and L= 20 mH. The value of switching frequency employed in the simulation for the healthy operation is equal to 5 kHz. The operation of MLIs at higher switching frequency reduces the filter size requirement which adds on benefits in the perspective of cost. The input voltage supplied to the ANPC topology is of magnitude 50V. The capacitors rating heavily influence the size and cost of the capacitors while practical implementation of the MLIs. Thus, by taking these factors into consideration and maintaining the quality of output voltage by appropriate charging and discharging, the rating of capacitors utilized is of 4700 micro Farad. The results obtained for five level output voltage waveform (a), output current waveform (b) and during this healthy operation is shown below in fig. 2(a) and fig.2(b). The capacitor voltage balancing can be observed from the figures of capacitors C1 and C2 voltage waveform during healthy operation as shown below in fig. 3(a) and (b):

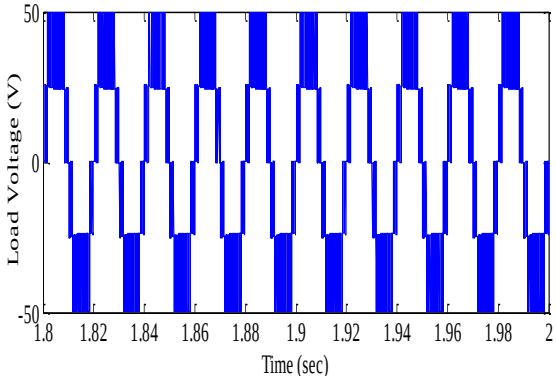

Fig. 2(a) Simulation results for output voltage waveform

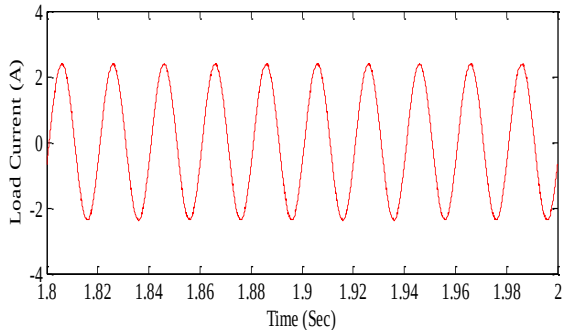

Fig.2 (b) Simulation results for output current waveform

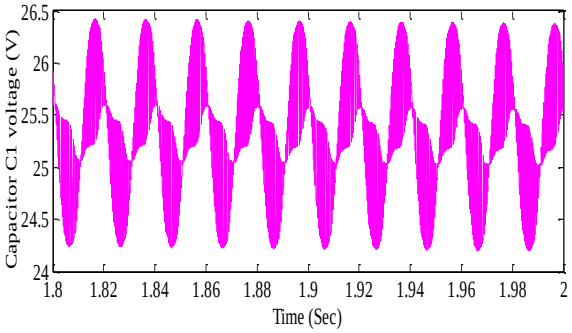

Fig. 3(a) Simulation results for capacitor C1 voltage waveform

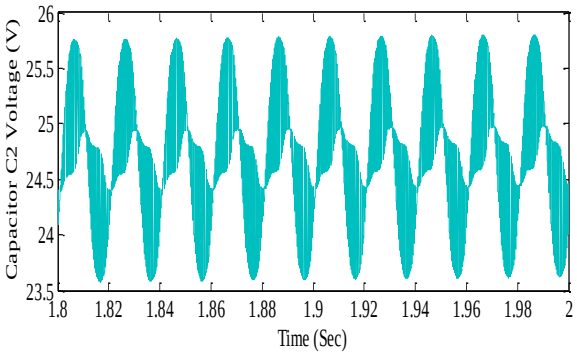

Fig. 3(b) Simulation results for capacitor C2 voltage waveform

In healthy operation of five level ANPC topology the above results are obtained with the corresponding switching scheme. This topology has eliminated the major issue of the non-uniform power loss distribution amongst the power switches, which yields to the uniform distribution of junction temperature amongst the main power switches. Thus, during the healthy operation of this topology the probability of failure in the power switches has greatly reduced. The capacitor balancing without implementation of control technique further reduces the cost of the inverter.

III. PROPOSED TOPOLOGY

The architecture of the proposed topology is shown in Fig.4. The proposed fault tolerant topology is developed by as the extension of conventional ANPC topology. The topology based on the conventional ANPC structure mainly focuses on the uniform distribution of power loss amongst all the power switches which is the major concern in case of the conventional NPC topology. The reduced count of the power electronics devices required to achieve the desired output is an extra advantage of the five-level ANPC topology. The proposed topology is developed to make the conventional five-level ANPC topology as fault tolerant with least number of additional power switches that can be utilized to achieve the required five level output voltage waveform. A1 to A6 for one leg and B1 to B6 for the second leg of the conventional ANPC topology are the primary path switches which produce a 5 level load voltage waveform under healthy mode of operation.

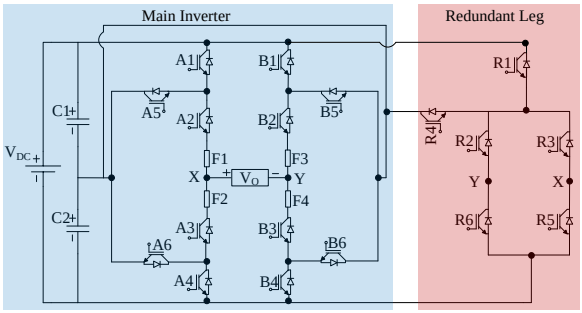

Fig 4.Architecture of proposed fault tolerant multilevel inverter topology.

To develop a fault tolerant topology the redundant leg switches have a unique position in the proposed topology which is based on two principle factors:

1. The dc-link capacitors voltage balancing by equally utilizing them under the faulty situation is only possible if both the capacitors have equal charging and discharging time during one full cycle.
2. Conduction losses are further decreased due to utilization of either one or two switches during the faulty duration to achieve the lost voltage levels, which will increase the efficiency of the inverter.

IV. PROPOSED SWITCHING SCHEME UNDER FAULTY CONDITION

The proposed fault tolerant topology is developed by the extension of conventional five-level ANPC topology. Thus, the switching strategy employed for the healthy operation of conventional ANPC topology will be same as that of the proposed fault tolerant multilevel inverter topology. However, after the open circuit fault analysis on every switch, the switching paths for the proposed fault tolerant topology during the open circuit failure condition on power switches A1 to A6 of single leg of three-level ANPC topology is shown in table-2. Since, the other leg of three-level ANPC is connected in parallel to the first leg the failure on switches B1 to B6 will also have same switching paths to generate desired load voltage levels. Thus, fault analysis for switches A1 to A6 for first leg will be similar to that of the switches B1 to B6. The lost voltage levels generation and capacitor balancing is achieved with the distinct position of main power switches of the redundant leg connected in parallel with five-level ANPC topology. Table-2 shown below comprises of the information regarding the relation between magnitude of pre fault and post fault voltage after the redundant leg comes into the operation. This table also consists of the information regarding the recovered voltage levels and the capacitor voltage balancing.

The pulses for gate signal are generated by the technique of level shift pulse width modulation (LS-PWM). These pulses are generated by the comparison of high frequency carrier signals and reference sinusoidal signal of fundamental frequency.

Table-2: Obtained output voltage level with the redundant leg in operation

OC faulty switch	Redundant leg active switches	Recovered output voltage level	Capacitor balancing ?	Output voltage:
A1	R1&R3	VDC	YES	YES
A2	(R1&R3) or (R1&R4)	VDC, VDC/2, -VDC/2	YES	YES
A3	R5, (R2&R3)	-VDC	YES	YES
A4	R5	-VDC	YES	YES
A5	R1&R4	N/A	YES	YES
A6	R3&R4	N/A	YES	YES

V. SWITCHING STRATEGY FOR RECOVERY OF LOST VOLTAGE LEVELS

The recovery of lost voltage levels due to fault on any one of the switches of first leg of five-level ANPC topology can be done with the redundant leg

in operation. Since, the second leg is connected in parallel with the first leg the fault analysis and switching strategy will be similar as that of the fault on first leg. The capacitor voltage balancing is possible because of availability of switching paths due to unique position of switches connected in redundant leg as shown in fig.4. The detail of operation of proposed topology with the fault on individual switches is described below.

V.1 For fault on switch A1

When open circuit fault occurs on switch A1, the lost voltage level V0=’VDC’ can be achieved through redundant leg. The voltage ‘sequence 1’ which is lost due to fault on switch A2 use switches A1, A2, B3 and B6, thus this voltage level can be generated with redundant switches having switching path R1, R3, B3 and B6. Since, the capacitor voltage balancing was not concern during fault on switch A1 no redundant switches are required to turn ON to generate corresponding voltage level. The switching path required to generate voltage level V0= ‘VDC’ is shown in the fig.6. given below. Thus the post fault voltage will be also gets equal to the pre fault voltage due to generation of this voltage level.

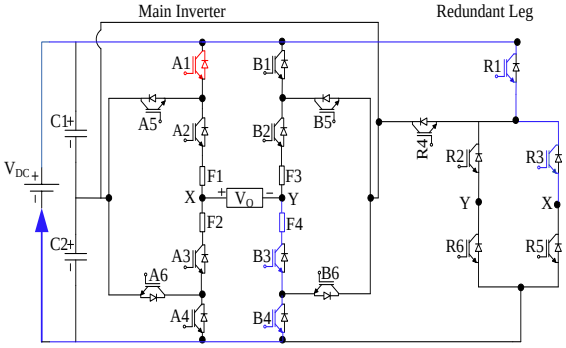

Fig.6. Switching path to generate voltage level VDC while fault occurs on switch A1

V.2 For fault on switch A2

Due to the open circuit fault occurring on switch A2, the lost voltage levels V0=’VDC’, V0=’VDC/2’, V0=’-VDC/2’, can be generated through redundant leg switches. The lost voltage ‘sequence 1’ due to fault on switch A2 which use switches A1, A2, B3 and B6 can be achieved with redundant switches with switching path R1, R3, B3 and B6 i.e. similar to the path shown in fig.6 given above. The capacitor voltage balancing concern during fault on switch A2 can be solved by generating the lost voltage sequence i.e. ‘sequence 2’ which primarily utilise switches A1,A2,B3 and B6 through another redundant path R1,R3, B3 and B6. This switching path generate voltage level V0=’VDC/2’, and discharges capacitor C1 and charges capacitor C2. Now, the one switching sequence i.e. sequence ‘11’ which uses switches A3, A4, B2 and B5 is already available to generate voltage level V0=’-VDC/2’, even after the occurrence of fault and has opposite impact on state of both the capacitors when compared to same voltage level generation with redundant switches during positive half cycle (i.e. VDC/2). Thus, the equal charging and discharging of capacitor will maintain the balancing with this strategy. Thus, required voltage level can be generated and the post fault voltage can be maintained equal to the pre fault voltage. Thus the post fault voltage will be also gets equal to the pre fault voltage due to generation of this voltage level. The lost voltage sequence 2 generation for voltage level V0=’VDC/2’ with redundant path is shown below. For the generation of same voltage level another redundant path switches R1 and R4 also can be utilized.

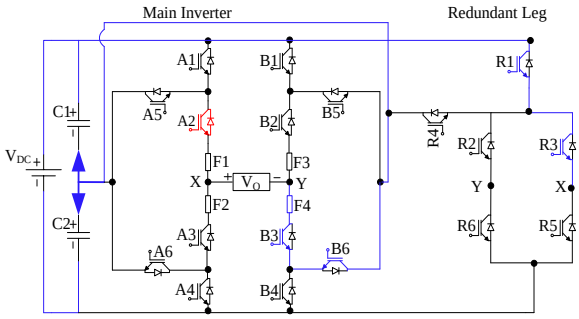

Fig.7. Switching path to generate voltage level VDC while fault occurs on switch A2

V.3 For fault on switch A3

Due to open circuit fault on switch A3, the lost voltage level V0=’-VDC’ can be achieved through redundant leg. The voltage ‘sequence 12’ which is lost due to fault on switch A3 use switches A3, A4, B1 and B2, thus this voltage level can be generated with redundant switches having switching path R5, B1 and B2. Since, the capacitor voltage balancing was not concern during fault on switch A3 no redundant switches are required to turn ON to generate corresponding voltage level. The switching path required to generate voltage level V0=’-VDC’ is shown in the fig. 8 given below. Thus the post fault voltage will be also gets equal to the pre fault voltage

due to generation of this voltage level. The same voltage level can also be generated with another available switching path due to redundant switches R2 and R3.

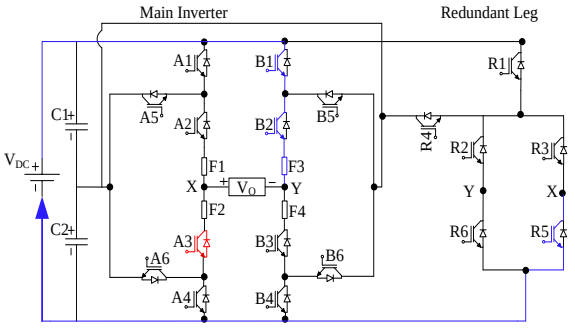

Fig.8. Switching path to generate voltage level VDC while fault occurs on switch A3

V.4 For fault on switch A4

The open circuit fault on switch A4, leads to the loss of voltage level V0= '-VDC' that can be achieved through redundant leg. The voltage 'sequence 12' which is lost due to fault on switch A4 use switches A3, A4, B1 and B2, thus this voltage level can be generated with redundant switches having switching path R5, B1 and B2. Since, the capacitor voltage balancing was not concern during fault on switch A3 no redundant switches are required to turn ON to generate corresponding voltage level. The switching path required to generate voltage level V0='-VDC' is shown in the fig.9 given below. Thus the post fault voltage will be also gets equal to the pre fault voltage due to generation of this voltage level.

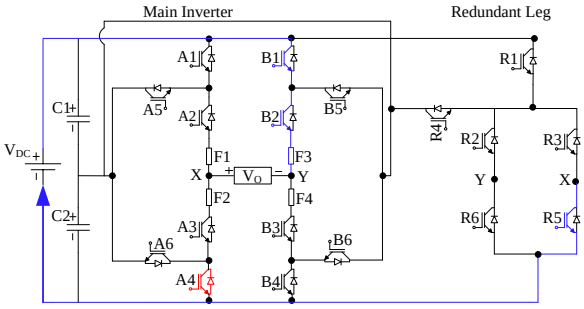

Fig.9 Switching path to generate voltage level VDC while fault occurs on switch A4

V.5 For fault on switch A5 and A6

Since no voltage levels are lost due to fault on switch A5 and A6 the redundant switches are not required to turn ON for this fault conditions. However redundant switches R1&R4 and R4 and R3 can be used as an alternative to recreate path for lost voltage sequences which will lead to the availability of all redundant paths. Thus the all voltage sequences can be generated with redundant leg in operation and the continuous healthy operation of inverter can be assured with the availability of all switching paths same as in pre fault condition.

VI. CONCLUSION

A novel fault tolerant topology which is an extension of five-level ANPC is proposed in the dissertation work. The topology generates a five level output voltage waveform in the healthy mode of operation and able to tolerate single switch faults. The topology is capable of maintaining the self-balancing of the dc-link capacitors due to the adopted switching scheme. The distinct positioning of switches in the redundant leg allows achieving single switch failure on semiconductor switches incorporated in the ANPC topology.

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