Implementation of Low Power and Area Efficient Vedic Multiplier using FinFET based Pass Transistor Logic

T.Mani[1], M.Sahira[2], G.Sathya Priya[3], M.Santhiya[4], K.Valuppural[5]
[1]*Assistant Professor, Dept of ECE, Jai Shriram Engineering College, Tirupur*
[2,3,4,5]*Final year, Dept of ECE, Jai Shriram Engineering College, Tirupur*

Abstract **- Designing a low power consuming and area efficient Vedic multiplier using Hybrid Full Adder. Arithmetic operations play on vital role in many real-time applications. Vedic multiplier has been introduced to solve the problems of existing multiplier. High speed and low power multiplier have been in increasing demand day by day. Multiplier like Array multiplier, Booth multiplier, Bit serial multiplier, Carry save multiplier and etc.., are used for as source of the algorithms. This algebra arithmetic operations and geometry. Urdhva Tiryabhyam is widely employed formula which provides high speed and efficient. This paper designs a Vedic multiplier with FinFET based pass transistor logic.2*2 and 4*4 Vedic multipliers are developed and executed 180nm approach with Tanner EDA Tool 3.0.**

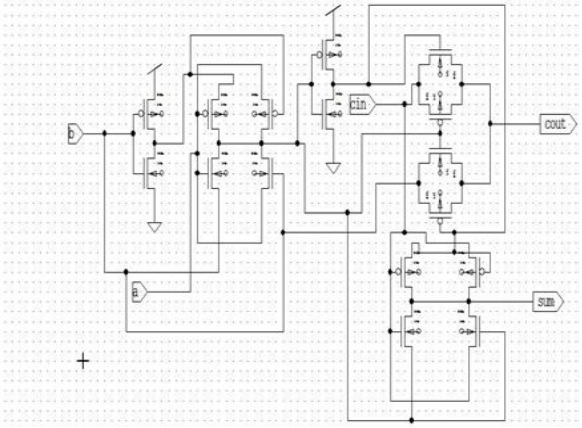
Index Terms **- Arithmetic operation, Algebra, FinFET, Vedic Multiplier.**

INTRODUCTION

CMOS technology dominates VLSI and other logic families. But this technology has some drawbacks which have been solved. For an instance, the process technology has reduced the size from 180nm in 1999 to 60nm in 2008. Now it is reduced to 45nm. Several attempts being made to reduce it 32nm. However, die area shrunk during 2008 now is increasing due to the greater number of transistors and its features. Vedic multiplies with different architecture is designed using carry save adder and ripple carry adder. Performances are compared and their merits and demerits are identified with respect to speed and area focused in Adiabatic logic is utilized to minimize power consumption of Vedic multiplier and its performance is estimated by comparing it with traditional MOS design Vedic multiplier with adiabatic logic consumes less power than Vedic multiplier without adiabatic logic analysed in. FinFET implies Fin Field Transistor. The power and zone productive plan of full adder with 6 transistors utilizing proposed 2 transistors XOR gate has been displayed. The pass transistor is used to decrease the transistor count for any implementation logics utilizing privacy input to drive gate terminals, source and drain terminals. Multiplies is an important component in digital signal processing (DSP) and communication systems. It is utilized in signal and image processing applications including convolution, Fast Fourier Transform (FFT) and correlation. Therefore, it is necessary to develop a multiplier with power efficient and speed to reduce the cost of the systems. It is based on 16 algorithms. The main advantage is the use of FinFET which provide numerous profits and advantages over the bulk CMOS.

II HYBRID FULL-ADDER

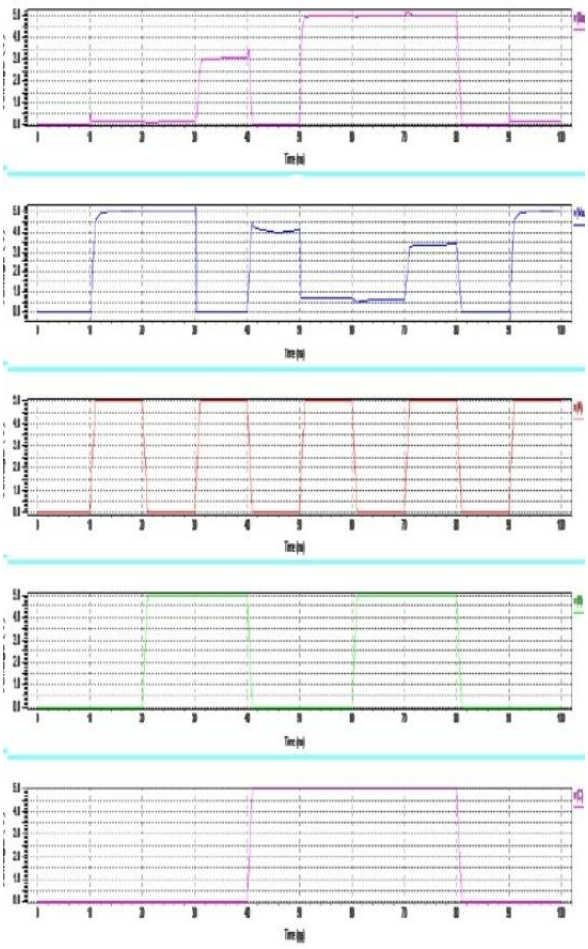
The hybrid logic has a module for carry generation using modified XNOR. In hybrid logic (small) conventional CMOS (CCMOS) and transmission gates are coupled together to obtain low power and high-speed operation. The XNOR module is designed with Conventional CMOS and the module to generate carry is designed using transmission gates.



Hybrid Full-Adder (Transistor level)

There are two modules that are present in the design of Hybrid XNOR module. To achieve faster conduction, the Weak inverter is used. The weak inverter consists of smaller depletion layer that helps in quicker conduction.

The wave form consists of three digital input and two analog input This input are given to the circuit and also output obtained from NMOS circuit.



Waveform of the Existing Full adder

In this Circuit we have analysed the following parameters from output wave form, Voltage vs. time, voltage, and current and frequency vs time the time scale is used in output circuit so that we can change input time period and, we have displayed the power and delay in the output waveform.

The implementation of 16-bitVedic Multiplier using CCMOS and Hybrid Full adders in Carry Save Adder block is carried out in Tanner EDA tool. The Area and Power Consumption calculations are done in 180nm Technology.

In the place of normal Full-Adders, these Hybrid Full-Adders are used in Ripple Carry Adders of the Vedic Multiplier. The hybrid logic has a module for carry generation using modified XNOR. In hybrid logic Conventional CMOS and transmission gates are coupled together to obtain Low power and High speed operation.

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Power Results
vdd from time 0 to 0.0001
Average power consumed -> 8.332886e-003 watts
Max power 1.709659e-002 at time 2.0001e-005
Min power 3.151799e-007 at time 9.00113e-005
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Hybrid Full Adder Power Calculation

The performance comparison of 16-bit Vedic Multiplier when executed by replacing Conventional Full-Adder with Hybrid Full-Adder has optimizes Area, Power Consumption.

From the simulated result using Tanner EDA tool the Power consumption of the existing logic styles are reduced by the proposed design.

III PROPOSED METHOD

Full-Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as Cin. The output carry is designated as Cout and normal output. The 10T Full adder designed with fusion of several XOR and modules. Half adder, full adder and AND gate is used to implement Urdhva Triyabhyam. In the following section, details of the above-mentioned components are discussed.

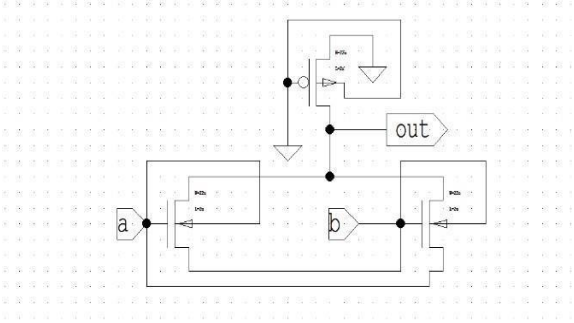
FinFET Technology

The Vedic multiplier is used to simplify the multiplication process and delay. If the Vedic multiplier is designed by using CMOS transistors, the circuit will raise problem. To overcome this issue, the Gate Diffusion Input (GDI) logic has been implemented using by FinFET technology.

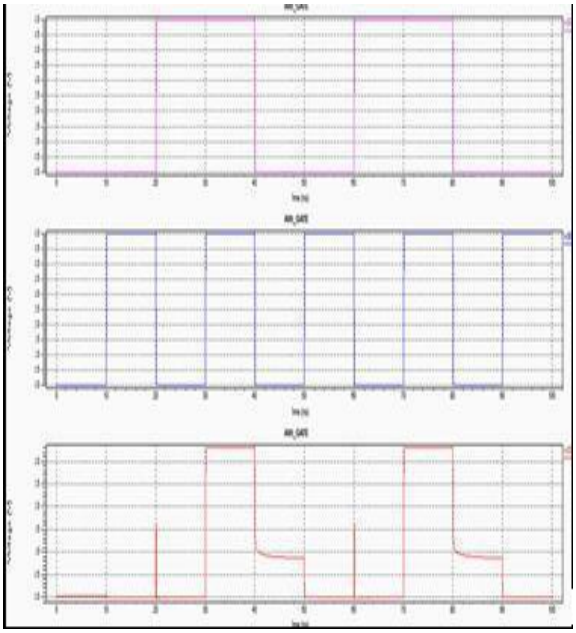
AND Gate

AND gate is an operation where the outputs become high/true when all the inputs are true and this AND gate can be a two input or multiple input based on the requirements. AND gate can be called a sequential

check gate i.e., if we want to check a condition in which two sequential signals should be true these the two input signals can be connected to AND gate and output of AND gate can be takes as controlling command.



The Proposed design of 3T-AND gate using SG-FinFET.

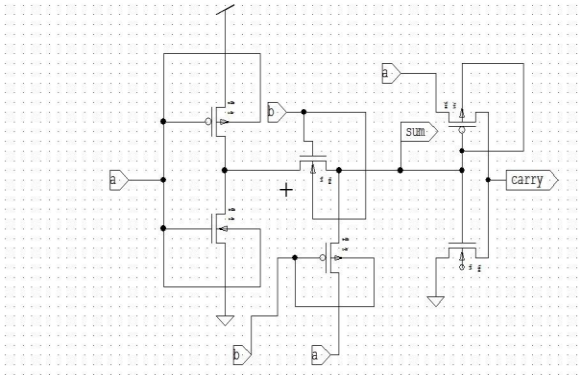


Stimulated Output Waveform for 3T-AND gate.

An optimized AND gate can be designed using FinFET Technology. In optimized 3T AND gate, first NMOS gate is joined to second NMOS source and vice versa. The inputs are fed to both the NMOS and output is observed via drain. PMOS terminals, gate and source are connected to ground.

Half Adder

Half adder designed by combination of logic gates, It is simple and developed utilizing and XOR and a multiplexer in which XOR produces the sum and the multiplexer produces the carry.10 transistor full Adder designed with fusion of several XOR and modules.



The Proposed design of 6T Half Adder using SG-FinFET

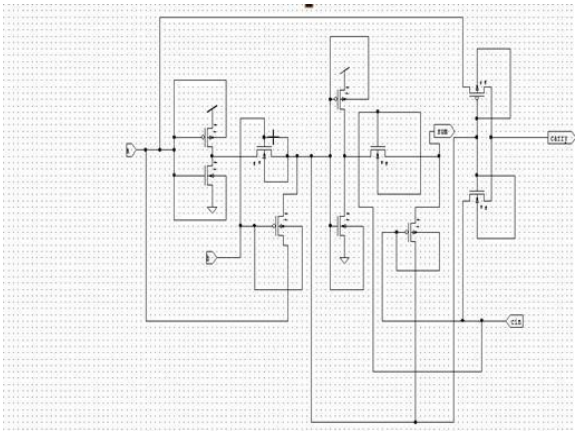
4T XOR gate is used to act as inverter whenever input B is at logic high then output of XOR is inverted form of A and whenever input B is at logic presented in Figure 3.6 and this when connected with multiplexer gives an half adder circuit. A schematic of 6T half adder where 4T XOR gate is to generate carry.

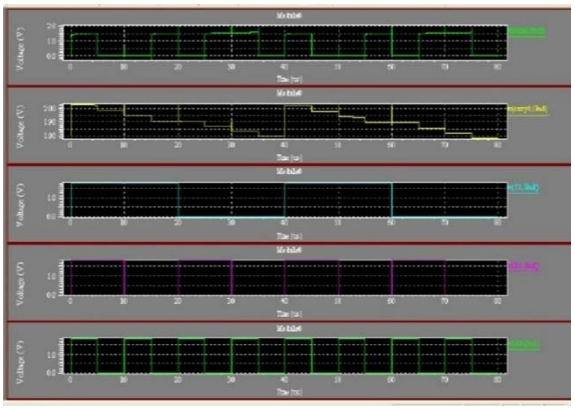
Stimulated graph for 10T Half Adder

When sum is high, then PMOS turns OFF and NMOS turns ON so output carry gives low (ground).

Full Adder

Full adder is the adder which adds three inputs and produces two outputs. The first two inputs area and band the third input is an input low PMOS turns ON and NMOS turns OFF so output carry is equal to A. The XOR circuit with four transistor is carry as cin. The output carry is Designated as cout and the normal output is designed in Such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another.



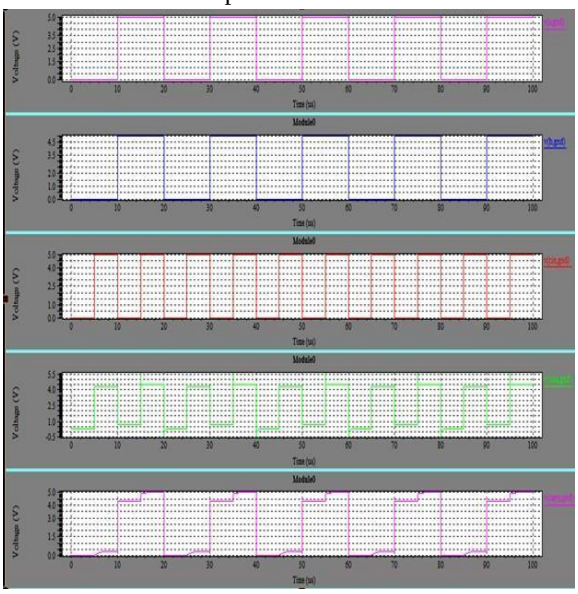


The Proposed design of 10T Full Adder using SG-FinFET

The above diagram shows the 10T full adder while 23T XOR gates are utilized which would produce sum and one 2TMUX is used which is controlled by the first two inputs which in return produce the carry. It operates as such than whenever inputs A and B are same then sum is equal to third input cin and carry is equal to A.

The waveform consists of three digital input and two analog input These inputs are given to the circuit and also output obtained from NMOS circuit .in this circuit, We have analysed the following parameters from output waveform, voltage vs time, Voltage and current, frequency vs time.

The proposed Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. On the other hand, we proposed a new architecture, which is efficient interms of speed.



Waveform of the proposed full adder

From the results, it is found that the proposed multiplier has the potential to reduce the delay. In literature, most of the Vedic multiplier has the structure of array. This paper presented architecture. The proposed architecture is efficient with respect to speed.

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Power Results
vdd from time 0 to 0.0001
Average power consumed -> 3.844713e+009 watts
Max power 7.688657e+005 at time 2.0001e-005
Min power 1.351777e-011 at time 5.5001e-005
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10T Full Adder using SG-FinFET Power Calculation. The time scale is used in output circuit so that we can change input time period and also we have displayed the power and delay in the output waveform. Whenever inputs A and B are different sum will be equal to inverted form of Cin and carry is equal to Cin.

IV CONCLUSION

The presented a comprehensive analysis for Vedic multiplier using Fin FET based Pass Transistor Logic (PTL). Two common structures of Vedic multiplier in hybrid full adder and Vedic multiplier using Fin FET based Pass Transistor Logic were analysed. Also based on theoretical analyses, a new Vedic multiplier with low-voltage low power capability was proposed in order to improve the performance of the Vedic multiplier. And the simulation outputs were shown with the help of the tanner software. The proposed multiplier is implemented on ISIM. The proposed architecture of Vedic multiplier is verified by software Tanner EDA Tool V13.0. Performance of the proposed Vedic multiplier is validated, and its operations are tested by observing experimental results. From the results, it is observed that the combinational delay is minimized with a tradeoff related to area. Change in power dissipation has been drastically reduced and this shows the success of this proposed design.

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